11-14-00

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	**2836- P056D1**
First Inventor	Alexander
Title	Circuits & Methods...Using the Same
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ Fee Transmittal Form (e.g., PTO/SB/17)
   (Submit an original and a duplicate for fee processing)

2. ☐ Applicant claims small entity status.
   See 37 CFR 1 27.

3. ☒ Specification [*Total Pages* 76]
   (preferred arrangement set forth below) copies from parent attached
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (*if filed*)
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure + Tables

4. ☒ Drawing(s) (35 U.S.C. 113) [*Total Sheets* 25]
   copies from parent attached

5. Oath or Declaration [*Total Pages* 3]
   copies from parent attached
   a ☐ Newly executed (original or copy)
   b ☒ Copy from a prior application (37 CFR 1.63 (d))
      (for continuation/divisional with Box 17 completed)
      i. ☐ **DELETION OF INVENTOR(S)**
      Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1 63(d)(2) and 1 33(b)

6. ☐ Application Data Sheet. See 37 CFR 1.76

7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)

8. Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
   a. ☐ Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i ☐ CD-ROM or CD-R (2 copies); or
      ii ☐ paper
   c. ☐ Statements verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☒ Assignment Papers (cover sheet & document(s)) copied from parent attached

10. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney copied from parent attached
    (when there is an assignee)

11. ☐ English Translation Document (*if applicable*)

12. ☐ Information Disclosure Statement (IDS)/PTO-1449   ☐ Copies of IDS Citations

13. ☒ Preliminary Amendment

14. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Other:

17. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

☐ Continuation   (☒ Divisional)   ☐ Continuation-in-part (CIP)   of prior application No 08 , 833,185

Prior application information.   Examiner Xu Mei   Group / Art Unit 2644

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation <u>can only</u> be relied upon when a portion has been inadvertently omitted from the submitted application parts.

18. CORRESPONDENCE ADDRESS

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Registration No. (Attorney/Agent)	34,503	
Signature	James J. Murphy	*Date* 11/13/00

FEE TRANSMITTAL
for FY 2001

Patent fees are subject to annual revision

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Alexander
Examiner Name	Xu Mei
Group Art Unit	2644
Attorney Docket No.	2836- P056D1

TOTAL AMOUNT OF PAYMENT ($) 710.00

METHOD OF PAYMENT

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to

Deposit Account Number: **23-2426**

Deposit Account Name: **Winstead Sechrest & Minick**

☒ Charge Any Additional Fee Required Under 37 CFR 1 16 and 1 17

☐ Applicant claims small entity status See 37 CFR 1 27

2. ☐ **Payment Enclosed:**
☒ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee ($)	Fee Code	Fee ($)		
101	710	201	355	Utility filing fee	710.00
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710.00

2. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims	40 -20** = 0	X	= 0
Independent Claims	5 - 3** = 0	X	= 0
Multiple Dependent			=

Large Entity		Small Entity		Fee Description
Fee Code	Fee ($)	Fee Code	Fee ($)	
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

**or number previously paid, if greater, For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee ($)	Fee Code	Fee ($)		
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	
146	710	246	355	Filing a submission after final rejection (37 CFR § 1 129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid   **SUBTOTAL (3)** ($) 0

SUBMITTED BY		Complete *(if applicable)*	
Name (Print/Type)	James J. Murphy, Esq.	Registration No (Attorney/Agent)	34,503
Signature	*James J. Murphy*	Telephone	214 745-5374
		Date	11/13/00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Alexander

Parent Serial No: 08/833,185

Parent Art Group: 2644

Parent Title: CIRCUITS AND METHODS FOR IMPLEMENTING AUDIO CODECS AND SYSTEMS USING THE SAME

Assistant Commissioner for Patents
Box Application
Washington, D.C. 20231

Dear Sir:

PRELIMINARY AMENDMENT

The present application is a divisional application of pending application Serial No. 08/ 833,185, filed April 4, 1997. Applicants respectfully request that the Examiner consider the following amendments and remarks. Please amend the application as follows.

IN THE TITLE

Please replace the title with A MULTIPLE STAGE ATTENUATOR.

IN THE SPECIFICATION

Amend the specification by inserting before the first line, the sentence:

CROSS REFERENCE TO RELATED APPLICATIONS

This is a division of application serial no. 08/833,185, filed April 4, 1997, (Attorney Docket No. 2836- P056US) entitled CIRCUITS AND METHODS FOR IMPLEMENTING AUDIO CODECS AND SYSTEMS USING THE SAME by Alexander, et al., Inventors, currently pending; and

Continuation application serial no. 09/631,924, filed August 3, 2000, (Attorney Docket No. 2836- P056C1) entitled CIRCUITS AND METHODS FOR IMPLEMENTING AUDIO CODECS AND SYSTEM USING THE SAME, by Alexander, et al., Inventors, currently pending.

IN THE CLAIMS

Please cancel Claims 1-18 and 24-40.

Please amend Claim 19.

19. (AMENDED)   An attenuator comprising:

a first stage comprising:

a first operational amplifier;

a tapped resistor having an input for receiving input data[.], an output coupled to an output of said first operational amplifier, and a plurality of taps for selectively presenting a sequence of voltages to said noninverting input of said operational amplifier, each of said sequence of voltages corresponding to an attenuation step, said first stage in response to said sequence of voltages stepping an attenuation produced by said attenuator from an intermediate value to a predetermined ending value; and

a second stage comprising:

a second operational amplifier;

a tapped resistor having an input for receiving analog data from said first stage, an output coupled to an output of said second operational amplifier, and a plurality of taps for selectively presenting a sequence of voltages to a

noninverting input of said operational amplifier, each of said sequence of voltages corresponding to an attenuation step, said second stage stepping said attenuation from a predetermined starting value to said intermediate value.

IN THE ABSTRACT

Please delete the title and abstract and insert:

A MULTIPLE STAGE ATTENUATOR

ABSTRACT:

An attenuator includes a first stage 601a having a first operational amplifier 602a and a tapped resistor 603a. Tapped resistor 603a has an input for receiving input data, an output coupled to an output of first operational amplifier 602a, and a plurality of taps for selectively presenting a sequence of voltages to a noninverting input of first operational amplifier 602a. Each of these sequences of voltages corresponds to an attenuation step such that first stage 601a steps the attenuation produced by the attenuator from an intermediate value to a predetermined ending value. A second stage 601b includes a second operational amplifier 602b and a tapped resistor 603b. Tapped resistor 603b includes an input for receiving analog data from first stage 601a, an output coupled to an output of second operational amplifier 602b, and a plurality of taps for selectively presenting a sequence of voltages to a noninverting input of operational amplifier 602b. Each of the sequence of voltages corresponds to an attenuation step, a second stage 601b stepping the attenuation from a predetermined starting value to the intermediate value.

REMARKS

The present application is a division of application serial no. 08/833,185, filed April 4, 1997, entitled CIRCUITS AND METHODS FOR IMPLEMENTING AUDIO CODECS AND SYSTEMS USING THE SAME by Inventors *Alexander, et al.*
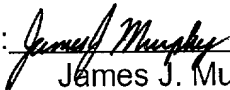
With the cancellation of Claims 1-18 and 24-40 and the addition of no new claims no additional filing fees are due. However, the Commissioner is hereby authorized to charge any fees or credit any overpayment to Deposit Account Number 23-2426 of WINSTEAD SECHREST & MINICK P.C.

If the Examiner has any questions or comments concerning this paper or the present parent and/or divisional application in general, the Examiner is invited to call the undersigned at (214) 745-5374.

Respectfully submitted,
WINSTEAD SECHREST & MINICK P.C.

By: _James J. Murphy_____
     James J. Murphy
     Registration No. 34,503

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Date: _November 13, 2000

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2836 P056D1

CIRCUITS AND METHODS FOR IMPLEMENTING
AUDIO CODECS AND SYSTEMS USING THE SAME

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates in general to digital
data processing and in particular to circuits and methods
5 for implementing audio Codecs and systems using the same.

DESCRIPTION OF THE RELATED ART

The ability to process audio information has become
increasingly important in the personal computer (PC)
environment. Among other things, audio is important in
10 many multimedia applications, such as gaming and
telecommunications. Audio functionality is therefore
typically available on most conventional PCs, either in
the form of an add-on audio board or as a standard
feature provided on the motherboard itself. In fact, PC
15 users increasingly expect not only audio functionality
but high quality sound capability.

One of the key components in most digital audio
information processing systems is the Codec
(coder-decoder) unit. Among other things, the Codec
20 converts input analog audio information into a digital
format for processing by a companion digital audio
processor. The digital processor for example may support
sample rate conversion, SoundBlaster compatibility,
wavetable synthesis, or DirectSound acceleration, among
25 other things. The Codec also converts outgoing signals
from the audio processor from digital to analog format
for eventual audible output to the user. The Codec may
also mix analog and/or digital audio streams.

Thus, to meet the demands of increasingly
30 sophisticated computer users, the need has arisen for new
circuits and methods for implementing audio Codecs, and
systems using the same. Among other things, such
circuits and methods should provide for the

implementation of Codecs for use with high quality sound systems and should support such features as stereo full-duplex coding/decoding, CD differential input, mono microphone input, and headphone output.

SUMMARY OF THE INVENTION

Audio data processing circuitry is disclosed which includes a plurality of analog inputs for receiving analog audio data and a digital input for receiving digital audio data. A first analog mixer is provided for mixing analog data received from the analog inputs to generate a mixed analog audio stream. An analog to digital converter converts the mixed analog audio stream to a digital audio stream. A digital mixer mixes the digital data received at the digital input with the digital audio stream from the analog mixer to generate a mixed digital audio stream.

The principles of the present invention substantially meet the demand of increasingly sophisticated computer users for audio subsystems which produce high quality sound. Additionally, the application of the principles of the present invention allows for the provision of such features as stereo full-duplex coding/decoding, CD differential input, mono microphone input, a headphone output, as well as digital connections to a companion audio controller, as desired.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1A is a diagram of the major components of a mixed-signal serial Codec according to the principles of the present invention;

FIGURE 1B is a more detailed overview diagram of the Codec of FIGURE 1A, which includes individual definitions of the inputs and outputs;

FIGURE 2A depicts the AC link connections between Codec and a digital AC '97 controller;

FIGURE 2B is a diagram illustrating the protocol for exchanging information between the Codec and controller depicted in FIGURE 2B;

5   FIGURE 3A is a more detailed diagram of a first embodiment of the mixer 300 of Codec 100 and the output and input cycles are generally illustrated in the conceptual timing diagram;

FIGURE 3B is an alternate embodiment 300B of the mixer section of Codec 100;

10   FIGURE 3C depicts another embodiment 300C of the mixer section of Codec 100;

FIGURE 4A is a diagram illustrating the bit fields of the Master Volume Control Register;

FIGURE 4B illustrated the bit fields of the

15   Alternate Volume Control Register;

FIGURE 4C is a diagram representing the bit fields of the Master Mono Volume Control Register;

FIGURE 4D is a diagram of the PC_BEEP Volume control register;

20   FIGURE 4E illustrates the Analog Mixer Input Gain Registers (Phone Volume, Mic Volume, Line-in Volume, CD Volume, Video Volume, Aux Volume, PCM Out Volume);

FIGURE 4G is a diagram of the General Purpose Register (Index 20h), the defined bits of which are the

25   MIX, MS, and LPBK bits;

FIGURE 4H is a diagram illustrating the bit fields of the Powerdown Control/Status Register;

FIGURE 4I is a diagram illustrating the bit fields of the Test Control Register;

30   FIGURE 4J is a diagram of the ADC/DAC Calibration Address Register;

FIGURE 4K is a diagram generally describing the bit fields of ADC Calibration Data Register, which is a vendor reserved readable/writable register used to

35   provide access to the ADC Calibration Registers;

FIGURE 4L is a diagram of the bit fields of the DAC
Calibration Data Register; and

FIGURE 5 is diagram illustrating a sequence of
operations occurring during start up (cold reset) of the
5   Codec;

FIGURE 6A is a diagram of a selected two stage
output volume/mute control (attenuator) 600;

FIGURE 6B is a schematic diagram of tap registers
the output amplifier of FIGURE 6A;

10   FIGURE 6C is a schematic diagram of a selected block
of the tap registers;

FIGURE 6D is a diagram depicting a selected one of
the decoders of a selected one of the tapped resistors;

FIGURE 7 is a diagram of the muting controls logic;

15   FIGURE 8 shows the pinout for Codec 100 for a 48-pin
TQFP package.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

        The principles of the present invention and their
advantages are best understood by referring to the
illustrated embodiment depicted in FIGURES 1-8
5   of the drawings, in which like numbers designate like
parts.

        FIGURE 1A is a diagram of the major components of a
mixed-signal serial Codec 100 according to the principles
of the present invention. As discussed further below,
10   when used in a system including a digital audio
accelerator (controller), Codec 100 mixes analog data
streams received from system-external sources and digital
data streams received from the controller. In addition
to embodying the principles of the present invention,
15   Codec 100 is also compliant with the Intel AC '97
specification, revision 1.03, September 15, 1996,
incorporated herein by reference.

        As shown in FIGURE 1A, Codec 100 includes input port
101 for receiving data from 4 mono and 4 stereo analog
20   input sources. Input multiplexer 102 selectively
presents one of the analog inputs received at input port
101 to analog to digital converters (ADCs) 103. After
conversion of the selected data stream from analog to a
digital format, that data is passed on to an audio Codec
25   (AC) Link driver 104.

        AC-Link 104 allows Codec 100 to communicate with the
companion digital controller via a 5-wire serial link
105. In accordance with the AC '97 specification serial
link 105 consists of 2 clock lines, 2 data lines, and a
30   reset line.

        The output path of a Codec 100 includes digital
analog converters 106, for transforming the digital data
processed by AC-Link 104 into an analog format, and an
output mixer 106. Output mixer 106 presents to the
35   output port 107 a stereo output, on two lines, and a mono
output on a single line. Signals output from output port

107 can then be recorded or delivered to audio components (amplifiers, speakers,...) for audible presentation to the user.

5   FIGURE 1B is a more detailed overview diagram of Codec 100, which includes individual definitions of the inputs into input port 101, lines 5-wire serial link 105, and the outputs from output port 107. Further, FIGURE 1B depicts selected internal data and control signals pertinent to the present discussion. FIGURE 1B also

10 generally shows the AC '97 registers 108, internal test circuitry 109 and power management circuitry 110.

   As shown in FIGURE 1A, the input port 101 is comprised of 8 individual inputs, 4 single line (pin) inputs for receiving mono source information and 4 two

15 line (pin) inputs for receiving stereo source information. The specific signals include LINE_IN, AUX_IN, VIDEO_IN, MIC1_IN, MIC2_IN, PHONE, and PC_BEEP.

   The LINE_IN pair of inputs provide for the input of left and right stereo analog data. The two AUX_IN inputs

20 provide left and right channel stereo analog auxiliary source input. The pair of inputs CD_IN are used for the input of left and right channel CD audio analog data. The input pair labelled VIDEO_IN are provided for inputting left and right channel stereo analog audio

25 signal inputs from a video device. Each of these inputs pairs are nominally $1V_{RMS}$, internally biased at the V_{REFOUT} voltage reference, and normally are AC coupled to the auxiliary analog source.

   Inputs MIC1_IN and MIC2_IN are multiplexed inputs

30 each of which can dependently be used as a monophonic analog input source to output mixer 106. The selected input also provided to the input mixer. These lines are provided as alternate microphone connections with the input nominally at $1V_{RMS}$, internally biased at the V_{REFOUT}

35 voltage reference, and are normally AC coupled to the respective input source.

The PHONE single-pin input provides for the input of data from a voice modem. The PHONE input is not coupled to the stereo to mono mixer. This input is nominally $1V_{RMS}$ internally biased at the V_{REFOUT} voltage reference and

5   is normally AC coupled to the external source circuitry.

The input (single-pin) labeled PC_BEEP provides a PC_BEEP connection to Codec 100. This input is also not coupled to the stereo to mono mixer. The input voltage is nominally $1V_{RMS}$ internally biased at the V_{REFOUT} voltage

10   reference and is AC coupled to the appropriate source circuitry.

5-Wire AC link 105 provides for the input of the synchronization (SYNC), data from the controller (SD_OUT) and reset signals, and for the output of link clock

15   (BIT_CLK) and data to the controller(SD_IN), as required to interface Codec 100 with digital AC '97 controller. FIGURE 2A depicts the AC link connections between Codec 100 and a digital AC '97 controller 200. Controller 200 could be any controller conforming to the Intel AC '97

20   specification. For example, controller 200 may be a Crystal Semiconductor CS-4610 device configured as an AC '97 controller. Such a device is described in detail in co-pending and co-assigned United States Patent Application Serial No. _____, ("Attorney

25   Docket Number 2836-P055US") entitled "Circuit, Systems and Methods for Processing Multiple Data Streams," filed February 7, 1997.

BIT_CLK is the main clock which defines the protocol used on link 105. This clock is generated by Codec 100

30   by dividing in half a 24.576 megahertz signal received from an external crystal (not shown) to obtain a 12.288 megahertz clock BIT_CLK. The BIT_CLK signal has a duty cycle between 40% and 60% and is used by controller 200 to synchronize signals SYNC and SDATA_OUT passed back to

35   Codec 100.

The signal SYNC is generated by controller 100 and presented to Codec 100 to define the beginning of a data frame. SYNC is a 48-khertz clock generated by dividing BIT_CLK by 256. The logic high period of this signal is

5   defined to be equal to 16 periods of BIT_CLK (approximately 1.3 microseconds) and is synchronous to the rising edge of BIT_CLK.

The signal SDATA_OUT (serial output data) is generated by controller 100 and input to Codec 100. In

10   particular, this data is positioned by controller 200 on the rising edge of BIT_CLK and Codec 100 samples this data on the falling edge of BIT_CLK.

SDATA_IN is used by controller 200 to receive serial data and status information from Codec 100.

15   Specifically, Codec 100 positions data on the SDATA_IN line on the rising edge of BIT_CLK and controller 200 samples of the signal transferred on this line on the falling edge of BIT_CLK.

Reset signal RESET is generated by controller 200

20   and forces Codec 100 into a power-on type initialization. In particular, in the active state, reset is held low for a minimum of 1 microsecond. Once RESET transitions to a logic high state, Codec 100 enters a normal mode of operation after a start-up delay to power-up the

25   reference voltages and calibrate the internal blocks.

Output port 107 includes an output pair LINE_OUT, ALT_LINE_OUT output pair and a single MONO_OUT line. The pair of outputs LINE_OUT are the left and right channel stereo outputs from output mixer 106. These outputs are

30   nominally $1V_{RMS}$ internally biased at the V_{REFOUT} voltage reference and are normally AC coupled to external circuitry. Typically, a 1000 pF NPO Capacitor couples these outputs (pins) to analog ground.

The pair of outputs labeled ALT_LINE_OUT are the

35   right and left channel alternate analog (headphones) outputs from output mixer 106. These outputs are also

nominally $1V_{RMS}$ internally biased at the V_{REFOUT} voltage reference, are normally AC coupled to the appropriate external circuitry, and are coupled to analog ground through a 100 pF NPO Capacitor.

5   The output labeled MONO_OUT is a single line (pin) monophonic output from output mixer 106 at $1V_{RMS}$ internally biased at the V_{REFOUT} voltage reference. This output (pin) is normally AC coupled to external circuitry.

10   In sum, the primary output (LINE_OUT) is available to drive a stereo audio device, such as powered speakers 201 on similar 10KΩ audio loads. In embodiments having an alternate output (ALT_LINE_OUT), capability is provided to provide connection to additional stereo 10KΩ

15   audio devices or simply an optional stereo output. In alternate embodiments having instead a HP_OUT output, capability is provided to drive a set of stereo headphones or similar 32Ω audio component. Finally, the PHONE output is provided to transfer data to a telephonic

20   speakerphone, handset or headset.

During each audio frame, data is passed both to Codec 100 from controller 200 (the "output cycle") and to controller 200 from Codec 100 (the "input cycle"). The output and input cycles are generally illustrated in the

25   conceptual timing diagram of FIGURE 2B. It should be noted that in this diagram, the timing relationships are only generally illustrated for brevity and clarity. For example, the actual number of BIT_CLK periods between the rising and falling transitions of each slot will vary in

30   actual applications, depending on the width of the slot.

The SDATA_OUT signal in FIGURE 2C represents the data being transferred from controller 200 to Codec 100 during the output cycle. When SYNC transitions active (logic high) and is sampled as active by Codec 100 on the

35   falling edge of BIT_CLK, both Codec 100 and controller 200 are synchronized to a new audio data frame. The data

on the SDATA_OUT pin at this falling edge of the bit
clock is the final bit data of the previous audio frame.
On the next rising edge of BIT_CLK, the first bit of slot
0 is sent to Codec 100.

5   The first slot of SDATA_OUT (slot 0) is a 16-bit
(tag) slot which contains information about the validity
of data for the remaining 12 slots. The first bit in
slot 0 (bit 15) is the 'Valid Frame' bit. This bit
indicates if any of the following slots (slots 1-11)

10   contains valid data. If this bit is a '1', at least one
of the other 12 slots contains valid data. If this bit
is a '0', the remainder of the frame can be ignored.

          The next four bits of slot 0 (bits 11-14) are 'Slot
Valid' bits. Bits 14-11 correspond to slots 1-4

15   respectively. If any of these bits is a 1, the
corresponding slot contains valid data during the frame.
Slot 0 bits 10-0 are reserved.

          The data presented to SDATA_OUT pin is shifted out
MSB justified, with the most significant bit of the

20   actual data in the MSB position of each 20-bit slot. In
any case where there is less than 20-bits of valid data
for a given slot (e.g. 18-bit PCM data in a 20-bit slot),
the trailing (least significant) bit positions of the
slot are filled with logic 0s by controller 100. For the

25   reserved slots, the bit positions are normally all filled
with logic 0s

          TABLE 1 defines the audio output frame slots. Slot
0 is the Tag Control Register. It is the 16-bit slot
which determines validity of all other slots, as

30   described above. Slots 1 and 2 are used as a "command
port" for accessing the mixer registers discussed later.
Generally, there are 64 defined 16-bit registers which
may be accessed through the 20 bits of Slot 1 as
described in TABLE 2.

35   Bit 19 of Slot 1 is a Read/Write bit. When this bit
is a 1, the transaction is to be a read. When the bit is

a 0, a write will occur. In both cases, register
accesses only occur when the Slot Valid bit corresponding
to Slot 1 (bit 14 of slot 0) is active.

Bits 18-12 of Slot 1 contain a 7-bit register index.
All registers are defined to exist at even-byte
addressable boundaries (implying bit 12 would always be
'0'), however this cannot be assumed; Bit 12 is simply
ignored, and not assumed to be either a '0' or '1'. Bit
positions 11-0 are reserved and are filled with logic 0s
from the controller 200.

Slot 2 is the Command Data Port for each frame of
SDATA_OUT. This slot is used to write data to the mixer
registers. The most significant 16 bits of the slot
(bits 19-4) contain a new 16-bit value to be written to
the selected register. Bits 3-0 are ignored, but always
contain 0s. For any write to a Mixer register, the write
is considered to be an 'atomic' access. In other words,
when the Slot Valid bit for Slot 1 is set, the Slot Valid
bit for slot 2 should always be set during the same audio
frame. This guarantees that no write access will be split
across 2 frames. If the access defined in Slot 1 is a
read, Slot 2 is completely ignored.

Slots 3 and 4 contain the digital audio (PCM) left
and right channel playback streams; Slot 3 contains the
left channel data, and Slot 4 contains the right channel
data. In Codec 100, the pulse code modulated (PCM)
playback data will be taken from the most significant 18
bits of Slot 3 and Slot 4, and the least significant 2
bit positions of these slots are ignored.

Slots 5-11 are reserved and the contents of their
bit positions are ignored, although 0s are preferably
written thereto by controller 100.

During an audio input cycle, data is transmitted
from Codec 100 output SDATA_IN to controller 200. The
format for the input cycles, as illustrated in FIGURES 3,
is similar to that of the output cycles. Synchronization

of Codec 100 and controller 200 is performed in the same manner, and the frame is again divided into 12 20-bit slots plus a single 16-bit Tag slot.

The first slot in the input cycle (Slot 0) serves two purposes. The most significant bit (Bit 15) is the 'Codec Ready' bit. This bit indicates the readiness of AC-Link 104 and the AC'97 Control and Status Registers. Immediately after a cold or power-on reset (discussed below) the Codec Ready bit is returned to controller 100 as a logic 0 and once the Codec clocks and voltages are stable, is transitioned to a '1'.

Bits 14-11 of Slot 0 are defined as 'Slot Valid' bits corresponding to the four data slots (Slots 3-6). When any of these Slot 0 bits are returned to controller 200 as a logic 1, the corresponding slot contains valid data. The remaining bits of slot 0 (bits 10 - 0) always return a logic '0' as they are reserved/undefined.

The audio input frame slot definitions are generally provided in TABLE 3. Slot 0, as described above, contains the 'Codec Ready' bits and 4 'Slot Ready' bits. Slot 1 is the Status Address Port. The Status Address Port allows controller 200 to access status and register data, including data in the mixer registers, from Codec 100. TABLE 4 defines the status address port bits of Slot 1.

The valid bits for Slot 1 are bits 18-12 which identify the index address of the register within registers 108 corresponding to the data being returned to the Status Data Port (Slot 2). All read operations are considered 'atomic' accesses. Therefore, the address of the register is returned in Slot 1 with the Slot 1 Valid bit set whenever read data are returned in Slot 2 with the Slot 2 Valid bit set.

Slot 2 is the "Status Data Port." Since all Mixer registers are 16-bits wide, the upper 16 bits (bits 19-4) of Slot 2 contain the contents of the register which was read in accordance with Slot 1, and the lower 4 bits

contain 0's. When Codec 100 is ready to return data
through this port, slot 0, bit 13 is set to 1. Data will
be returned from a read access on the frame following the
read request in all cases.

5   Slot 3 and Slot 4 are the PCM Record Data slots.
Codec 100 is a 18-bit Codec, and therefore will output to
controller 200 18-bit PCM data in the most significant 18
bit positions (bits 19-2) of the PCM Record slots. Bits
1-0 of both slots will always contain 0's. Slot 3
10   corresponds to the Left Channel data, while Slot 4
corresponds to the Right Channel data.

          Slots 5-11 of each frame of SDATA_IN are
reserved/undefined, and therefore will always return 0's
for all bits. Slot 5 could be assigned to carry modem
15   data when an optional modem is used and Slot 6 could be
used to carry optional microphone data, when a direct
microphone connection is provided (FIGURES 3A and 3B).

          FIGURE 3A is a more detailed diagram of a first
embodiment of the mixer 300A of Codec 100. The
20   individual components/subsystems are controlled by the
contents of corresponding registers within register 108,
as discussed further below. A design of the digital
portions of Codec 100 and in particular the digital
components of the system of FIGURE 3 is provided in
25   Appendix A. The data provided in Appendix A is the
Cadence Verilog hardware description language now in the
art, and may be executed on a Sun Microsystems (SPARC)
workstation.

          Codec 100 includes multiple processing paths for
30   mixing and converting data being exchanged between
controller 200 and external analog audio devices. Each
of these will be discussed in detail; however, the Codec
100 data paths can generally be described as follows.
During the input of data to controller 200, selector 102
35   selects one stream from among a set of streams including
the unmixed input analog streams (MIC1 or MIC2, LINE_IN,

CD, VIDEO and AUX_IN) and a mixed stream generated by
mixing these analog streams together and/or with PCM data
returned from controller 200. The selected stream, in
digital format, is transmitted to controller 200 via the

5   SDATA_IN line of link 105. During the output of data
streams from controller 200 to external audio devices,
PCM data from controller 200 is selectively mixed with
the audio input streams (MIC1 or MIC2, LINE_IN, CD, VIDEO
and AUX_IN), converted into analog format, and output to

10   the given external audio devices via the LINE_OUT,
MONO_OUT or ALT_LINE_OUT pins. Codec 100 further
includes a number of other selectable paths for
processing flexibility, including paths for specifically
processing data received through the PC_BEEP and PHONE

15   analog inputs.

        In one input path, MIC1 or MIC2, LINE, CD, VIDEO
and/or AUX input data presented at input 101 are passed
to input multiplexer 102 directly. Specifically, a
switch 301 allows the user to select for input between

20   data generated by microphone 1 (MIC1) or microphone 2
(MIC2). The selected microphone input is then amplified
by amplifier 302 by approximately +20 dB. The microphone
analog data output from amplifier 302 is presented not
only to the input of input multiplexer 102, but also

25   through an amplifier 303 and a dedicated microphone
analog-to-digital converter 304. The direct data path
through amplifier 303 and ADC 304, when used allows the
transmission of PCM microphone data to controller 200 via
the SDATA_IN line using one of the reserved frame slots.

30   The digitized (PCM) microphone input data from
analog-to-digital converter 304 is then sent to
controller 200 via the SDATA_IN link using a selected one
of reserved slots in each frame, such as Slot 6.

        The remaining signals, LINE, CD, VIDEO and/or AUX

35   are provided directly to multiplexer 102. Multiplexer
102 can thus select directly from any one of the signals

presented at input 101. Input multiplexer 102 has
independent control of the left and right channels which
advantageously facilitates returning a mono mix of the
stereo line channel and/or echo cancellation on the

5   microphone source by controller 200. In addition to
selecting any one of the five analog input sources, such
as MIC, CD, LINE_IN, VIDEO, or AUX, presented at inputs
101, multiplexer 102 can also select from the stereo
output mix or mono output mix discussed further below.

10   The input stream selected by input multiplexer 102
is amplified by amplifier 305 which in turn drives main
analog analog-to-digital converters 103. Each analog to
digital converter (ADC) discussed herein is generally a
delta-sigma ($\Delta\Sigma$) converter. After analog-to-digital

15   conversion, the two-line stereo input stream is passed
through mute control circuitry 306 and on to digital
mixer 307. It should be noted that each of the digital
mixers shown in FIGURES 3A-3C are digital adders with
saturation to prevent wrap around. Mixer 307 is provided

20   to mix the input signals selected by multiplexer 102 with
mixed digital stereo data tapped from the stereo mixing
section. The PCM formatted digital data output from
digital mixer 307 is transmitted to controller 200 via
AC' 97 link 105 on Slots 3 and 4 of the SDATA_IN stream.

25   The data received from the stereo mixing section by
digital mixer 307 results from the mixing of PCM data
received through the SDATA_OUT line of AC' 97 link 105
with the MIC1 or MIC2, LINE, CD, VIDEO, and AUX inputs of
input port 101. Specifically, the analog input signals

30   are input through corresponding volume controls 308a -
308e and mute controls 309a - 309e. Generally each input
volume/mute controls to Codec 100 are active tapped
alternators with zero crossing detection for volume
control update. Volume controls 308 and mute controls

35   309 are controlled by setting bits in the mixer registers
discussed below. Similarly, the PCM data from controller

200 is input through volume controls 310 and mute
controls 311, each of which is also controlled by bits
written into the mixer registers. The analog inputs MIC1
or MIC2, LINE, CD, VIDEO, AUX are then mixed by an analog

5   stereo effect mixer 312 before conversion to digital
format by effects path A-D converter 313. Each of the
analog mixers depicted in FIGURES 3A-3C are active
resistor summers. Additional mute controls 314 are
provided at the output of analog-to-digital

10   converter 313.

       A digital mixer 315 selectively mixes the outputs of
analog-to-digital converter 313 with the digital data
(serially left and right channel data from Slots 3 and 4
of SDATA_OUT) received from controller 200 through volume

15   control 310 and mute control 311. If mixing of PCM data
with the mixed and converted analog data from the analog
inputs is not desired before 3-D processing, only the
converted analog input data is passed through mixer 315.
The digital mixed signal output from mixer 315 can

20   optionally undergo 3-D audio processing by 3-D audio
circuitry 316 or can bypass 3-D processing circuitry 316
through switch 317. 3-D digital audio circuitry 316
performs such processing as volume control, reverb, pan,
Doppler, HRTF or similar audio enhancement options under

25   industry available protocols, such as SRSQX.

       Another digital mixer 318 provides an optional path
for mixing received data from controller 200 with the
data input from inputs 101. In this case, the mixing of
the data originally input as analog at inputs 101 is

30   mixed with the digital data direct from controller 200
after optional 3-D processing by 3-D processing circuitry
316. In other words, 3-D processing for the PCM data can
be selectively foregone, notwithstanding the fact that
3-D processing is performed on the converted analog input

35   data. The output of mixer at 318 is then provided to
tone controls 319. Tone controls when provided, provide

for adjustment of the bass and treble components, for
example in 1.5 dB or 3 dB steps. The two-channel output
of tone controls 319 are passed through mute controls 320
and directly therefrom to digital mixer 307.

5   The two-channel output of tone control 319 is also
provided to main digital-to-analog converter 106. The
digital to analog converters (DACs) of Codec 100 may be
for example a delta-sigma converter. Analog output from
main digital-to-analog converter 106 is passed through

10   mute controls 321 and on to analog stereo output mixer
322. Analog stereo output mixer 322 mixes the analog
signal output from main digital-to-analog converter 106
with the PC_BEEP and PHONE inputs received from input
port 101 (through volume controls 323a - 323b and mute

15   controls 324a - 324b). Mixer 322 can also receive analog
data directly from analog effects mixer 312 through a 90
dB analog bypass path. In particular, the analog bypass
path takes analog data directly from analog stereo
effects mixer 312, passes them through mute controls 325

20   and directly on to analog input mixer 322.

          Mixed analog output data from analog mixer 322
provides a further input to input multiplexer 102. Most
importantly, the output of analog stereo output mixer 322
passed to the LINE_OUT and HP_OUT outputs of Codec 100

25   output port 107 for transmission to external audio
devices. The LINE_OUT output is driven by master volume
control 327 and output buffer 328 while the HP_OUT output
is driven by headphone volume control 329 and headphone
driver 330. For the embodiment of FIGURE 3A, the

30   LINE_OUT designed to drive a load of approximately 10KΩ
and the HP_OUT designed to drive a load of approximately
32Ω

          The mono output (MONO_OUT) is not directly generated
from analog stereo mixer 322. Instead, a mono output

35   mixer 326 mixes in the PC_BEEP and PHONE sources with the
PCM and analog sources. This scheme is advantageous, for

example, because the mono mix from the mono output port may be used to drive a phone handset. Mixing the phone input back into the handset may cause echoes at the other end of the phone line. Therefore, the mono mix is taken

5   from the analog input mixer 312 through the analog bypass, which does not include the PC_BEEP or PHONE source signals. The MONO_OUT port is designed to drive an approximately 10K load.

FIGURE 3B is an alternate embodiment 300b of the

10   mixer section of Codec 100. In this embodiment, the direct microphone path to controller 200 via SDATA_IN comprising volume control 303 and analog-to-digital converter 304 has been eliminated. Additionally, mute controls 306 in the stereo PCM path to controller 200 are

15   not used in this embodiment. Further, the direct connection between mono output mixer 326 and multiplexer 102 has been replaced by a connection from analog output mixer 322 through an additional mixer 335. Mixer 335 takes the left and right stereo output from analog output

20   mixer 322 and mixes those channels to a single mono channel which is passed to multiplexer 102. Additionally, in this embodiment, as well as the embodiment of FIGURE 2B, the HP_OUT path has been replaced with a path for driving an approximately 10KΩ

25   load (i.e. ALT_LINE_OUT)

FIGURE 3C depicts another embodiment 300c of the mixer section of Codec 100. In this embodiment the PCM data from controller 200 is first converted from digital to analog by main digital analog converter 106. The

30   analog data output of D/A converter 106 is mixed with the analog inputs MIC1 or MIC2, LINE, CD, VIDEO, and/or AUX. The analog output of mixer 322 in turn mixes the analog output from mixer 312 with the PHONE and PC_BEEP analog inputs. The output of analog output mixer 322 then

35   directly passed to the volume controls 327 and 329 and output buffers 328 and 330, respectively driving the

LINE_OUT and ALT_LINE_OUT outputs of Codec analog output port 107.

The two-channel output of analog stereo output mixer 322 is mixed into single channel mono by mixers 326 and 335, respectively, with mixer 326 providing mono analog data to switch 333 and mixer 335 providing mono analog data to multiplexer 102.

TABLE 5 generally describes registers 108 of Codec 100. These registers include the "mixer registers" for controlling the various functions of mixer section 300, vendor identification registers, the Powerdown/Status register, and a General Purpose register. The bit names in TABLE 5 will be defined in conjunction with the discussion in FIGURES 4A -4L and the individual registers themselves. Bit positions denoted with an 'X' are reserved. As such, writes to these positions are ignored and reads are returned with undefined values. Bit positions denoted with a '0' indicate values which are hard-coded to logic '0' values. Thus, writes will not change the values in these register positions, and they will always read as '0's.

The reset register is shown in TABLE 5 and is located at index 00h. Any write to this register causes a register reset, forcing all Mixer Control Registers to return to their default state. Reads from the Reset Register will return configuration information about Codec 100 identifying any optional features which are supported. For example, in embodiments of Codec 100 which support the 18-bit DAC/ADC as well as the Headphone Output (Alternate Line Out), the read value from this register will be 0150h.

FIGURE 4A is a diagram illustrating the bit fields of the Master Volume control register at register index 02h. The Master Volume control register is used to control the LINE_OUT signal volume by master volume controls 327, with each register step corresponding to

1.5 dB volume adjustment across a range of 0 dB to 94.5 dB of attenuation. The most significant bit (MSB) of this register controls a master analog mute for the LINE_OUT output. Bits ML5-MLO of the register are used to control Left Channel Volume and bits MR5-MR0 are used to control the Right Channel Volume. The default value for the Master Volume control register is 8000h, corresponding to 0 dB attenuation and mute on.

The bit fields of the Alternate Volume control register (Index 04h) are illustrated in FIGURE 4B. The Alternate Volume control register is used to control ALT_LINE_OUT signal volume through volume controls 329. Each register step corresponds to 1.5 dB volume adjustment in a range between 0 dB and 94.5 dB of attenuation. The MSB of this register controls a master analog mute for the ALT_LINE_OUT. Bits ML5 - MLO of the register are used to control the Left Channel's volume, and bits MR5-MR0 are used to control the Right Channel's volume. The default value for this register is 8000h, corresponding to 0 dB attenuation and mute on.

FIGURE 4C is a diagram representing the bit fields of the Master Mono Volume control register (Index 06h). The Master Mono Volume control register is used to control the MONO_OUT output volume in conjunction with mono volume controls 331. Each register step corresponds to 1.5 dB volume adjustment over a range 0 dB to 94.5 dB of attenuation. The MSB of this register controls a master analog mute for the MONO_OUT output. Bits MM5 - MMO of the register are used to control the actual volume levels. The default value for this register is 8000h, corresponding to 0 dB attenuation and mute on.

A Master Tone control register is included at register index 08h. This register provides for tone adjustment by tone controls 319, when provided.

FIGURE 4D is a diagram of the PC_BEEP Volume control register (Index 0Ah). The PC_BEEP Volume control

register is used to control the mix of the PC_BEEP signal into Analog Output Mixer 322 by volume controls 323a and mute controls 324a. Each register step corresponds to 3.0 dB volume adjustment across a range of 0 dB to 45 dB of attenuation. The MSB of this register controls a master analog mute for the PC__PEEP and bits PV3 - PV0 control the actual volume levels. The 4 data bits PV3-PV0 are not aligned to the least significant bit position of the register. In other words, data bit 0 (PV0) corresponds to bit D1 of the register. The 3 dB steps in volume control with each step of the value (PV3-PV0) differ from all other gain controls, which provide a 1.5 dB precision. The default state of the mute bit (bit D15) is a '0', meaning that mute is disabled on power-up.

The Analog Mixer Input Gain Registers (Phone Volume, Mic Volume, Line-in Volume, CD Volume, Video Volume, Aux Volume, PCM Out Volume at indices OC-18h, respectively) are illustrated in the diagram of FIGURE 4E. These registers control the gain levels of the analog input sources to the Input Mixer 312 by volume controls 308 and 310 and mute controls 309 and 311. Each register step for all registers corresponds to 1.5 dB gain adjustment, thus allowing a range of 12 dB to -34.5 dB of gain. The MSB of these registers control an analog mute for each source to input mixer 312. Bits Gx4-Gx0 of each register are used to control the gain levels of the corresponding source. The gain mapping for these bits is shown in TABLE 6.

Register 0Eh (the Mic Gain Register) has one additional defined bit, bit D6, which is used to enable the 20 dB gain, which is available for either MIC source, through amplifier 302. Specifically, when bit D6 set to a logic '1', 20 dB gain block 302 is enabled. The default values for the mono input source registers (0Ch and 0Eh) are 8008h, corresponding to 0 dB attenuation and mute on. For the stereo source registers (10h through

18h), the default values are 8808h, corresponding to 0 dB attenuation for both channels with mute on.

5   The Input Mux Select control register (Index 1Ah) is used to direct multiplexer 102 to pass a source signal received at its inputs to main analog to digital converters 103 for recording. As discussed above, multiplexer 102 is allows for independent control of the left and right channels received from each source. Bits SL2 - SL0 provide the decode for the left channel input

10 and bits SR2-SR0 provide the decode for the right channel input. The default power-on value for this register is 0000h, selecting the MIC inputs for both channels. A decode of the bits stored in the Input Mux Select control register is given in TABLE 7.

15 The Record Gain Register (Index 1Ch) controls the input gain of amplifier 305 disposed after input multiplexer 102 and before analog to digital converter 103. The 4 bit value loaded into this register provides a control range of +22.5 dB to 0 dB of gain. The most

20 significant bit of the register controls an analog Mute which mutes the signal prior to ADC 103. TABLE 8 illustrates the possible gain values available. The default value for this register is 8000h, which corresponds to 0dB gain with mute on.

25 The Record Gain Mix control register (Index 1Eh) is used to control the gain of amplifier 304 to the MIC PCM input, when used. This register and amplifier 304 function in a manner similar to that of the Record Gain Register discussed above.

30 FIGURE 4G is a diagram of the General Purpose Register (Index 20h), the defined bits of which are the MIX, MS, and LPBK bits. The MIX bit selects which data to send to the Mono Output Path (MONO_OUT). Specifically, a logic '0' passes the output of mixer 326

35 through switch 333 to MONO_OUT while a logic '1' passes the previously selected MIC signal to the output. The

MIC Select bit (MS) determines which of the 2 MIC inputs
are passed to the rest of mixer section 300 through
switch 301. A '0' selects MIC 1 Input, while a '1'
selects MIC 2 Input. Finally, the LPBK bit enables an
5   ADC/DAC Loopback Mode to facilitate performance
evaluation of the mixer path.

The 3D Control Register (Index 22h) allows for
control of 3D audio processing circuitry, in those
embodiments where the 3D feature is provided.

10   The Modem Rate control register (Index 24h) is
provided for user rate control when an optional Modem
connection is included.

FIGURE 4H is a diagram illustrating the bit fields
of the Powerdown Control/Status Register (Index 26h).
15   TABLE 9 generally describes the function of each of the
Powerdown Status Bits while TABLE 10 generally describes
the function of each of the Powerdown Control Bits. The
PR7 and MDM are provided for optional modem features.
Specifically, PR7 provides powerdown capability for a
20   Modem processing subsection and the MDM bit indicates
whether that Modem subsection of the Mixer is ready upon
powerup.

The Reserved Registers (at Indices 28h-58h) are
reserved and therefore writes to these registers are
25   ignored and read values from these registers are always
0000h. The Revision and Fab ID Register indicates the
revision level of the device as well as the fabrication
facility where the part was manufactured. The Vendor ID
register indicates the distributer and/or producer of the
30   part.

FIGURE 4I is a diagram illustrating the bit fields
of the Test Control Register (Index 5Ch). This Vendor
Reserved register is used to control Test Mode entry.
The test mode bits (bits T3-T0) chose from one of 12
35   possible test modes available. The discussion below
describes the various test modes.

FIGURE 4J is a diagram of the ADC/DAC Calibration
Address Register (Index 76h). This Vendor Reserved
register controls access to the ADC and DAC calibration
registers. The upper byte of the calibration address

5   register (bits 15-8) is used to access the ADC
Calibration registers, and the lower byte (bits 7-0) is
used to access the DAC Calibration registers. This
register can be read at any time, but to write new
calibration values to the registers requires entry into a

10   vendor specific test mode. To read either bytes of this
register, a write is made to the appropriate register
index selected from those set forth in TABLES 11 and 12.
Specifically, TABLE 11 generally describes the ADC
Calibration Register Address Mapping (bits A1-A0) and

15   TABLE 12 generally describes DAC Calibration Register
Address Mapping (bits D1-D0). To perform a write, the
register index is set along with at least one of two
write enable bits WEA and WED. As soon as any access
(read or write) occurs to the Calibration Data register,

20   the Write Enable bit associated with that register is
cleared to prevent accidental writes. Writes can be
performed to both registers during a single access. The
default value for this register is 0000h and when read,
the unused bits will always return 0's.

25   FIGURE 4K is a diagram generally describing the bit
fields of ADC Calibration Data Register (Index 78h),
which is a vendor reserved readable/writable register
used to provide access to the ADC Calibration Registers.
When a valid index is set in the ADC/DAC Calibration

30   Address register discussed above, a read to the ADC
Calibration Data Register will return the most
significant 16 bits of the 19-bit available bit
positions. When Codec 100 is in test mode 0xf (discussed
below) and the WEA bit of Register 76h is set, a write

35   will update the selected ADC Calibration Data Register.
The write will place the 16-bit value in the upper 16-

bits of the ADC Calibration register, and fill the lower
3 bits with zeroes. When WEA is set, any access, read or
write, to this register will clear the WEA bit
automatically. If the A1-A0 index bits of register 76h

5   are set to either '00' or '11', this register will return
an undefined value.

        FIGURE 4L is a diagram of the bit fields of the DAC
Calibration Data Register (Index 7Ah). This
readable/writable vendor reserved register is used to

10   access the DAC Calibration Registers. When a valid index
is set in the ADC/DAC Calibration Address register, a
read to the DAC Calibration Data Register will return the
most significant 16 bits value of the 19-bit available
bit positions. When Codec 100 is in test mode 0xf and

15   the WED bit of Register 76h is set, writes will update
the selected DAC Calibration Register. Specifically, the
write will place the 16-bit value in the upper 16-bits of
the DAC Calibration register, and will fill the lower 3
bits with zeroes. When WED is set, any access, read or

20   write, to this register will clear the WED bit
automatically. If the D1-D0 index bits of register 76h
are set to either '00' or '11', this register will return
an undefined value.

        As previously described, the Powerdown

25   Control/Register provides for individual powerdown of
different sections of Codec 100. TABLE 13 more
particularly describes the bit mapping for the powerdown
GPR Bit Functions. Selected functions can also be
described as follows.

30   When, for example, the PRO is set, the ADC bit (bit
0 in register 26h) is cleared to '0' to indicate the ADCs
103 are no longer in a ready state. The same is true for
DACs 106/312, Analog Mixers 312/322 and the Reference
Voltage (Vref) generator. When the PR bit corresponding

35   to one of the sections of Mixer 300 is cleared back to
'0', that section will begin a power-on process, and the

corresponding Powerdown Status bit will be set ready
('1') when the hardware is in a ready state.

Assertion of Bit PR4 (logic "1"), causes the AC-Link
105 to turn off the BIT_CLK and drive SDATA_IN to a '0'.
The SYNC and SDATA_OUT inputs are ignored by Codec 100.
To restore operation to the part from this state, either
a cold or a warm reset is required. A cold reset will
restore all Mixer registers to their power-on default
values. A warm reset will not alter the values of any
Mixer register (with the exception of clearing the PR4
bit of register 26h).

Bit PR5 is a 'global powerdown of the Codec' bit.
When set, all internal clocks of Codec 100 are shut down.
A cold reset is thereafter required to re-establish
communications with the Controller 200 since the AC-Link
clock is deactivated when Bit PR5 is set.

Codec 100 does not automatically mute any input or
output when the powerdown bits are set. The software
driver controlling device therefore manages the muting of
the input and output analog signals before putting Codec
100 into any power management state. Internal to Codec
100, there are multiple powerdown control signals for
various portions of the chip. TABLE 14 generally
describes the relationship of each of these signals to
the powerdown control bits.

The PDN_DAC is used to powerdown main DACs 106/335.
DACs 106/335 can be powered down whenever the Mixer,
internal clock, or the DAC powerdown signals are set.
The PDN_ADC bit is used to similarly powerdown the ADCs
103 whenever Vref, the internal clocks, or the ADC
powerdown bits are set. The PDN_MDC signal is used to
powerdown analog mixer 322 whenever the internal clocks
or the Mixer powerdown bits are set.

Signal PDN_REF is used to powerdown the internal
voltage reference generation (Vref) circuit whenever the
Vref or internal clocks powerdown bits are set.

PDN_BITCLK disables the external BIT_CLK clock. This
occurs whenever the AC-Link or the internal clock
powerdown bits are set. PDN_ALT_LINE is used to
powerdown the Alternate Line Output buffer 330 whenever

5   analog mixer 322 is powered down, the internal clocks are
disabled, or the explicit Headphone Powerdown bit is set.
PDN_CLK256_INT stops the internal BIT_CLK (256Fs) clock.
This will only occur when the internal clock disable
powerdown bit is set PR5).

10   When no activity is occurring across the link 105,
Codec 100 can be operated in a low power mode.
Specifically, a Powerdown Control/Status register Index
(0x26) of registers 109 bit 12 is set to a logic '1' and
link 105 is powered down. Codec 100 drives both BIT_CLK

15   and SDATA_IN to low levels immediately after the write to
register and the remainder of the current audio frame is
ignored. At the same time, controller 200 drives the
SYNC and SDATA_OUT signals to logic low levels. In this
state, the data SDATA_OUT is ignored

20   Codec 100 supports 'cold reset' and 'warm reset
modes to returning AC '97 link 105 to full power up. A
cold reset is performed when Codec 100, including its
registers, is initialized to its default state. A warm
reset is performed when the contents of the registers of

25   Codec 100 are to remain unaltered.
             Controller 200 initiates a cold reset by asserting
the RESET# signal. Once controller 200 has deasserted
RESET#, all of the registers of Codec 100 will have been
reset to a default power-on state and the BIT_CLK and

30   SDATA_IN signals will be reactivated. Additionally, If
the PR5 bit (bit 13) of the Powerdown Control/Status
register 0x26 is set to a logic "1" then a 'cold reset'
is require. Generally, a cold reset follows the
following sequence of steps:

35   1.   Controller 200 sets RESET# low for a
                  minimum of 1uS (one microsecond);

2.   Codec 100 enters full power-down state;

3.   The Codec 100 mixer registers reset to default values;

4.   SDATA_IN and BIT_CLK signals on link 105 are held low by Codec 100;

5.   Controller 200 then reasserts RESET# high;

6.   The crystal oscillator (not shown) is powered up;

7.   The "Reference Voltage" charge phase begins;

8.   The Codec 100 internal power-on reset (POR) signal activated;

9.   A clock-off detector within Codec 100 indicates that the crystal oscillator has started (but may not be stable);

10.   Crystal oscillator stabilization timeout begins;

11.   Codec 100 starts BIT_CLK after crystal oscillator timeout completed (approximately 42.7 mS);

12.   The Codec 100 SYNC detect circuit is activated;

13.   When Codec 100 detects valid SYNC signal for 2 consecutive frames, Codec 100 begins valid data transmission on the next valid frame boundary, with the Codec Ready bit set to a logic '1';

14.   Voltage Reference charges up to 80%; Codec 100 internal POR (power on reset) signal goes inactive;

15.   170.7mS (millisecond) timeout for Vref charge phase begins following deassertion of Codec 100 internal POR;

16.   The REF bit of Codec 100 register 26h set to a logic '1' after 170.7mS timeout (2^{21} cycles of internal 256Fs clock);

17.   Codec 100 Auto Calibration begins
following 170.7mS timeout;
18.   Op-Amp calibration completes -ANL (analog
mixers, mux and volume controls ready) bit of
register 26h set to a '1' (~128 frames);
19.   ADC calibration completes in approximately
200 frames;
20.   DAC calibration completes in approximately
-88 Fs frames);
21.   ADC (ADC 103 ready to accept data) bit of
register 26h set to a '1' and DAC (DAC 106
ready to transmit data) bit of register 26h set
to a '1'; and
22.   Normal operation begins.

A warm reset is recognized when SYNC signal is
driven active (high) when the bit clock (BIT_CLK) is not
active on link 105. The SYNC signal is held high for at
least 1uS and SYNC is interpreted as an asynchronous
input to Codec 100. Once SYNC has been held high for the
required time, controller 200 drives SYNC low and Codec
100 activates bit clock BIT_CLK, typically after at least
2 normal BIT_CLK periods after Codec 100 samples SYNC low
(typically at least 162.8 nS). A warm reset generally
follows the following sequence:
1.   Controller 200 sets bit PR4 of Codec 100
register 26h (power Control/Status register) to
a '1';
2.   Codec 100 transitions SDATA_IN and BIT_CLK
to logic '0's within 1uS after Slot 2 of the
SDATA_IN stream completes;
3.   Codec 100 register states are frozen;
4.   Controller 200 signals a warm reset by
setting SYNC to a logic '1' for at least 1uS;
5.   Codec 100 detects warm reset after 1uS and
resets bit PR4 (Powerdown Control/ Status

Register) to a logic '0' when SYNC returns to a logic '0';

6.   Codec 100 starts BIT_CLK a minimum of 2 BIT_CLK periods (162.8nS) after falling edge of SYNC;

7.   Codec 100 SYNC detect circuit activated;

8.   Codec 100 detects valid SYNC signal for 2 consecutive frames, and begins valid data transmission on the next valid frame boundary, with the Codec Ready bit set to a logic '1'; and

9.   Codec 100 returns to normal operation, with registers set exactly as before bit PR4 in the Powerdown/Status register was set.

FIGURE 5 is a state diagram describing synchronization (sync) of Codec 100 with controller 200 and digital 105. The sync logic of Codec 100 is based upon an 8-bit counter which increments by one from 0 to 255 in response to BIT_CLK. The expected sync signal EX_SYNC remains in a logic high state as long as the counter maintains a count in the range of 1 to 17. When the signal INSYNC transitions high Codec 100, controller 200 and link 105 are synchronized ("in sync"). INSYNC transitions high when INSYNC_ST is a 2 or a 3. INSYNC_ST is a 2 or 4 bit state variable. If Codec 100 is in sync but EXSYNC is not equal to INSYNC, then a sync-error bit is set. \

A link protocol violation and/or loss of SYNC can occur if: (1) SYNC not sampled high for exactly 16 BIT_CLK cycles at the start of an audio frame; (2) SYNC not sampled high on the 256th BIT_CLK after the previous SYNC assertion; or (3) SYNC goes active high before the 256th BIT_CLK after the previous SYNC assertion. Advantageously, Codec 100 performs the following sequence of events to handle the situation:

1.   When loss of SYNC is detected, the
LINE_OUT mutes are enabled;

2.   SDATA_IN is transitioned to a logic '0' on
the next rising edge of BIT_CLK and will remain
a logic '0' until synchronization with
controller 200 is restored;

3.   SDATA_OUT is ignored and the Mixer
registers are frozen;

4.   A SYNC detect circuit begins looking for a
rising edge of SYNC;

5.   Once detected, the SYNC detect circuit
looks for 2 valid audio frames of SYNC clocks;

6.   When the second valid SYNC is detected,
Codec 100 assumes the link is again
operational;

7.   The LINE_OUT Mutes are disabled;

8.   The Codec Ready bit is set back to a logic
'1'; and

9.   Normal operation is restored on the
following audio frame.

The automatic setting of the LINE_OUT mutes do not
override the settings in the Mixer Control Registers.
The Mixer Register settings must remain as they were
before the loss of SYNC once synchronization is restored.
To facilitate this, Mutes should be implemented as shown
FIGURE 7.

FIGURE 6A is a high level functional diagram of a
two stage output volume/mute control (attenuator) 600.
Output volume/mute control 600 may be used to construct
master volume control 327, headphone volume/mute controls
329 or mono volume/mute controls 331. For a mono output
only one attenuator is required and for stereo outputs
two are required; one for each channel. Advantageously,
while volume/mute control 600 is a multiple stage device
(two stages are shown for brevity and clarity), to users

external to Codec 100, volume/mute control 600 appears to
be a single stage attenuator.

5

As shown in FIGURE 6A, a given attenuator 600
includes first and second stages 601a and 601b connected
in series. The first stage includes an operational
amplifier 602 and a 32-bit tapped resistor 603 for
controlling the voltage at the non-inverting input of the
corresponding operational amplifier 602. The inverting
input of each operational amplifier 602 is tied to a

10

reference voltage V_{cn}. Resistors 603 are digitally
controlled as discussed above.

Data is input to stage 601a and output to stage
601b, with operational amplifier 602b driving the output
(i.e., the output buffers, such as 328, 330, and 332 are

15

essentially merged into attenuators 600). The second
stage, stage 601b, provides for 0 dB to -48 dB of
attenuation in -1.5 dB steps. From then on, attenuation
is added by first stage 601a. Specifically, first stage
601a steps the attenuation from -48 dB to -94.5 dB in

20

-1.5 dB steps.

A zero crossing detector 604 is provided at the
input of second stage 601b. Zero crossing detector 604
is used to enable attenuator stages 601a and 602b when
signals are being output.

25

Multiple stage attenuator (volume/mute control) 600
has substantial advantages over existing single stage
attenuators. Among other things, second stage 602 is
able to attenuate any noise output from first stage 601a.
Additionally, by using multiple stages, each with an

30

independent tapped resistor, the consumption of die area
is substantially reduced. In particular, a single stage
amplifier for providing a comparative attenuation levels
would require the use of large resistors, each of which
consume significant die space.

35

As shown in FIGURE 6A, each stage has 32 bit tap
register 603. Tap registers 603a and 603b are identical,

each including 32 attenuation taps 605 as shown in FIGURE
6B. Thirty-two select bits SEL[31:0] are received from
decoding the bits in the output volume control register
for the corresponding output being driven. One tap of
5   one block 605a is selected to set the attentuation level
in steps of -1.5 dB. Each individual block 605 is
controlled by a unique 8-bit subset of the 32 select bits
received.

FIGURE 6C is a more detailed schematic diagram of a
10   selected block 605. As shown in FIGURE 6C, each block
605 includes a series of resistors 606. Corresponding
tap points are controlled by a transistor 607, the gate
of which is in turn controlled by a corresponding one of
the 8 select bits corresponding to the given block 605.
15   A transistor 608 is provided to turn off the output. The
output OUTP of each block 605 is either cascaded to the
next block 605 in the chain, or is coupled to the output
of the corresponding operational amplifier 602a or 602b.
The output OUTP of blocks 605 are cascaded and
20   subsequently coupled to the non-inverting input of the
given operational amplifier. The value of the resistance
of each resistor 606 correspondingly increases starting
with the resistor 606h of block 605d and similarly
continues increasing through the serial chain of
25   resistors block 605c, 605b and 605a. Block 605a is
received from the remainder of Codec 100 in the case of
stage 602a and from the output of first stage 601a in the
case of second stage 601b as required to set attenuation
steps of 1.5 dB.

30   FIGURE 6C shows for discussion purposes block 605d
whose output OUTP is coupled to the output of the
operational amplifier through an output resistor 609 to
the output of the operational amplifier as 602a or 602b.
Also assume for discussion that the selected tap point is
35   within block 605d shown in FIGURE 6D. The select byte
(SEL [7:0] in the case of block 605d) turns on one of the

transistors 607 so that the corresponding tap point in
the string of series resistors is coupled to the
non-inverting input of the corresponding operational
amplifier 602. For example, if the tap point selected is

5   between resistor 606a and 606b, at this tap therefore the
resistance will be the sum of all of the resistance
values of the resistors in blocks 605a, 605b and 605c
plus the resistance value of resistor 606a.
Consequently, the voltage at the non-inverting input of

10   given up amplifier 602 is the value of the input voltage
received at the input to block 605a multiplied by the
series resistance between the input of block 605a and the
tap point divided by the input impedance of the
operational amplifier 602.

15   FIGURE 6E is a schematic diagram depicting a
selected one of the decoders of a selected one of the
tapped resistors 603. Each tapped resistor 603 has 32
decoders similar to that shown in FIGURE 6E, with each
such decoder programmed to select one tap out of the

20   thirty-two taps available in the given amplifier 601a or
602b.

           For discussion purposes, FIGURE C depicts a decoder
for selecting tap number ten of the given tapped resistor
603. In particular, the programming of each decoder is

25   effectuated by the interconnections between the input,
inverter array composed of inverters 610, and an array of
transistors 611. Decoding is enabled by applying an
logic 1 (pdb) to the gate of transistor 612. Loading and
output drive capability is provided by transistor

30   613-616.

           In the example of FIGURE 6E, the inverters are
appropriately disconnected or not connected to ensure
that when a logic 10 (010100) is received, all
transistors 611 turn on which pulls down on the gates of

35   transistors 616a and 616b. The output is then driven to
approximately Vdd (logic 1) through load transistors 615.

The output then becomes part of the 32-bit word passed on
to the tapped resistor network. In this example, because
of the interconnections of the inverters 610 and 611 of
the thirty-one other select lines of the select bus

5   SEL[31:0] are in a logic low state.

Table 24 describes the coding inputs to decoders
603a and 603b. As previously stated, second stage 601a
introduces an attenuation of 0 to -48 dB and attenuator
stage 1 601a continues stepping the attenuation up to

10   -94.5 dB. When the most significant bit is set to 0,
stage two provides all the attenuation and data simply
passes through stage one. The inputs to each decoder 603
are provided by the volume/mute control register (TABLE
5) corresponding to the given output line (i.e.,

15   LINE_OUT, HB_OUT, AUX_OUT, or MONO_OUT). As shown in
TABLE 4, the increment by one least significant bit
corresponds to a step of -1.5 dB. When the most
significant bit is set to 0, stage two 601b provides
attenuation in the range of 0 dB (select = 00000) to

20   -46.5 dB (select = 11111). When the most significant bit
is set to 1, stage 2 provides an attenuation of -48 dB
and remains at that attenuation level as long as the most
significant bit is set to 1. Further, when the most
significant bit is set to a logic 1, stage 1 adds

25   attenuation to the -48 dB attenuation provided by stage
2. Specifically, stage 1 adds from 0 dB (select = 10000)
to -46 dB (select = 11111). Thus, for example, when
select = 11111, the total attenuation provided is -94.5
dB.

30   The primary test modes are defined in the following
TABLE 15. A write to the least significant 4 bits (bits
T3-T0) in register 5Ch (Test Modes) with the appropriate
test mode identifier will send Codec 100 into that test
mode. When test modes 2, 3, 4, or 10 are entered, a cold

35   reset is required to return the chip to normal operation,
or to enter another test mode. When a test mode is

entered AC-Link 105 remains fully active. Codec 100 will
enter a primary test mode if SYNC is sampled high (logic
'1') when RESET# is deasserted. If both SDATA_OUT and
SYNC are high when RESET# deasserts, this is a fault
5   condition, and no test mode is entered. Once a test mode
is entered, a cold reset is issued to restore normal
operation.

        The ADC 1-Bit Left Channel Data Test connects the
output of the left channel ADC Delta Sigma Modulator of
10   main ADCs 103. to the SDATA_IN pin. Similarly, the ADC
1-Bit Right Channel Data Test connects the output of the
right channel ADC Delta Sigma Modulator of Codec 100 to
the SDATA_IN pin. These two tests allow the 1-bit data
generated by the modulator for each channel to be probed
15   externally during analog test.

        The DAC 1-Bit Left Channel Data and DAC 1-Bit Right
Channel Data Tests respectively connect the output of the
left channel and right channel DAC Modulators to the
SDATA_IN pin. This allows the 1-bit data generated by
20   each modulator to be observed by test equipment external
to Codec 100, providing an digital test of the DAC for
each channel.

        The Analog and Digital Wrap Test breaks the
connections between the DAC Modulators and Switch
25   Capacitor Filters within main DACs 106 and between the
Delta Sigma Modulators and the ADC 103 Decimation Filters
within main ADCs 103. Then, the outputs of the DAC
Modulators are connected to the inputs of the ADC
Decimation Filters to facilitate a digital wrap test.
30   Likewise, the outputs of the ADC Delta Sigma Modulators
are connected to the inputs of the DAC Switch Capacitor
Filters for an analog wrap test.

        The Disable Zero Cross Detect test bypasses the ZCD
(zero cross detect) circuitry in the volume control
35   registers. This allows instant updates of volume
settings for any analog volume control registers. The

Zero-Cross Detection Test disables the slow clock to the ZCD circuitry.

Test Slow Counters changes the clock to the volume control time-out counters from an Fs clock to a 256Fs clock to facilitate test of the slow counters.

The Test Op-Amps test allows each op-amp to be connected to the MONO_OUT output such that all op-amps can be externally tested. This is done by writing a single bit somewhere in the mixer control registers. When this write occurs, any previous op-amp which was connected to the output is disconnected, and the newly selected op-amp is connected. For each op-amp, the assigned bit is different. Whenever possible, a bit which controls the gain for a particular op-amp is used. The mapping list is provided in TABLE 16

The NAND Tree Enabled test forces outputs of BIT_CLK and SDATA_IN to be connected to the output of a NAND Tree which consists of SYNC with SDATA_OUT. This facilitates V_{ih} and V_{il} testing.

When asserted, Disable Calibration automatic calibration is disabled for all analog sections of Codec 100.

When Force Op-Amp Calibration is set, all op-amps in the analog mixer begin calibration.

When Force ADC Calibration is set, the stereo ADCs in the analog mixer 322 begin calibration.

The Force DAC Calibration initiates calibration of the DACs in analog mixer 322.

Enable Cal Register Writes: When the test mode register is set to mode 0xf, write access to the Calibration registers is enabled. In other words, the protocol of using Codec Mixer registers 0x76, 0x78, and 0x7A to write new values to the Calibration registers is enabled. Whenever the test mode register bits are any other pattern than 0xf, writes will not be allowed to the Calibration registers.

Codec 100 further provides for the testing of
selected optional features. For example, Codec 100 will
enter an ATE modem in circuit test mode if SDATA_OUT is
sampled logic high ('1') when RESET# is deasserted

5   (driven high).

The pinout for Codec 100 is shown in FIGURE 8 for a
48-pin TQFP package. This package provides a 4.5mm x
4.5mm cavity for the die. TABLE 18 is a tabular listing
of the pins and corresponding signals.

10   TABLE 19 generally describes the functions of the
digital I/O pins for Codec 100. The analog source and
sink pins are likewise described in TABLE 20.

The filter and Reference pins are those pins which
are normally connected to external resistors, capacitors,

15   or specific voltages. TABLE 20 generally sets forth the
Filter and Reference Voltage pins.

TABLE 21 generally describes the power supply and
ground connections to Codec 100. Codec 100 is capable of
running the Digital Interface at either 5.0V or 3.3V.

20   The analog subsection is normally always run at 5.0V.

The DC characteristics for AC Link 105 are set forth
in TABLE 22. The AC characteristics for Codec 100,
including those of the signals supporting AC Link 105 are
generally described in TABLE 23.

25   It is therefore, contemplated that the claims will
cover any such modifications or embodiments that fall
within the true scope of the invention.

WHAT IS CLAIMED IS:

1.   Audio data processing circuitry comprising:
        a plurality of analog inputs for receiving analog
audio data;

5   a digital input for receiving digital audio data;
        a first analog mixer for mixing analog data received
at least some of said plurality of analog inputs to
generate a mixed analog audio stream;
        a first analog to digital converter for converting

10   said mixed analog audio stream to a digital audio stream;
and
        a first digital mixer for mixing digital data
received at said digital input with said digital audio
stream from said first analog mixer to generate a mixed

15   digital audio data stream.

2.   The processing circuitry of Claim 1 and further
comprising:
        a digital to analog converter for converting said
mixed digital audio data stream into an analog data

20   stream; and
        a second analog mixer for mixing said analog stream
received from said digital to analog converter with
analog data received directly from a selected said analog
input.

25   3.   The processing circuitry of Claim 2 and further
comprising a multiplexer for selecting between analog
data received from a one of said plurality of analog
inputs and analog data output from said second analog
mixer.

4.   The processing circuitry of Claim 3 and further comprising a second analog to digital converter to converting analog data received from said multiplexer to digital form for output.

5   5.   The processing circuitry of Claim 4 and further comprising a second digital mixer for mixing digital data output from said second analog to digital converter with digital data received from a tap point disposed prior to said digital to analog converter.

10   6.   The processing circuitry of Claim 1 and further comprising a least one output port for outputting analog data received from said second analog mixer.

7.   The processing system of Claim 6 and further comprising volume controls coupling said second analog
15   mixer and said output port.

8.   The processing system of Claim 7 wherein said volume controls comprise a two stage digitally controlled attenuator.

9.   The processing system of Claim 1 and further
20   comprising a processing path coupled to a selected one of said plurality of analog inputs, said processing path including an independent analog to digital converter and an output for selectively outputting digital data from said independent analog to digital converter to an
25   external device.

10.   The processing circuitry of Claim 1 and further
comprising 3D audio processing circuitry for selectively
receiving and processing digital data from said first
digital mixer.

5   11.   The processing system of Claim 10 and further
comprising a third digital mixer for alternatively mixing
digital data from said first analog to digital converter
with digital data received from said digital input port
subsequent to selective 3D processing of said data from
10   said first analog to digital converter.

12. An audio codec having multiple selectable processing paths comprising:

a first processing path comprising:

an analog input mixer for mixing analog data streams received at a plurality of analog inputs into an mixed analog data stream;

an analog to digital converter for converting said mixed analog data stream into a digital data stream;

a digital mixer for mixing data from a digital input with said digital data stream to produce a mixed digital data stream;

a digital to analog converter for converting said mixed digital data stream into a second analog stream;

an output mixer for mixing said second analog stream with analog data received from a second analog input, to produce an analog output stream; and

at least one output for transmitting said analog output stream to an external device; and

a second processing path comprising:

an multiplexer for selecting a data stream from among said analog streams received at said plurality of inputs and said output analog output stream;

an analog to digital converter for converting said selected data stream output by said multiplexer into digital form; and

an output port for transmitting said selected data stream in digital form to an external device.

13. The codec of Claim 12 and further comprising a third processing path comprising:

an analog to digital converter in parallel with said multiplexer for converting an analog data stream from a selected one of said plurality of analog inputs into digital form; and

an output for transmitting said stream in digital form to an external device.

14. The codec of Claim 12 wherein said first processing path further comprises 3D processing circuitry for processing digital data output from said at digital mixer.

15. The codec of Claim 14 and further comprising a second digital mixer for optionally mixing said digital data stream from said input mixer with digital data from said digital input subsequent to 3D processing of said digital data stream from said input multiplexer.

16. The codec of Claim 12 wherein said second processing path includes a digital mixer for mixing data output from said analog to digital converter of said second path with digital data received from a tap in said first processing path.

17. The codec of Claim 12 wherein said output port of said first path includes volume and mute controls and an output buffer.

18.   The codec of Claim 17 wherein said volume and mute controls and output buffer comprise:

a first stage comprising:

an operational amplifier;

a tapped resistor having an input for receiving analog data from said analog output mixer, an output coupled to an output of said operational amplifier, an a plurality of taps for providing a sequence of voltages to a noninverting input of said operational amplifier, said each voltage of said sequence of voltages corresponding to an attentuation step by said first stage in a range from an intermediate value to a predetermined ending value; and

a second stage comprising:

an operational amplifier;

a tapped resistor having an input for receiving data from said first attenuater mixer, an output coupled to an output of said operational amplifier, an a plurality of taps for providing a sequence of voltages to a noninverting input of said operational amplifier, said each of said sequence of voltages corresponding to an attentuation step by said second stage in a range from a predetermined starting value to said intermediate value.

19.   An attenuator comprising:
      a first stage comprising:
            a first operational amplifier;
            a tapped resistor having an input for receiving
      input data. an output coupled to an output of said
      first operational amplifier, and a plurality of taps
      for selectively presenting a sequence of voltages to
      said noninverting input of said operational
      amplifier, each of said sequence of voltages
      corresponding to an attentuation step, said first
      stage in response to said sequence of voltages
      stepping an attenuation produced by said attenuator
      from an intermediate value to a predetermined ending
      value; and
      a second stage comprising:
      a second operational amplifier;
            a tapped resistor having an input for receiving
      analog data from said first stage, an output coupled
      to an output of said second operational amplifier,
      and a plurality of taps for selectively presenting a
      sequence of voltages to a noninverting input of said
      operational amplifier, each of said sequence of
      voltages corresponding to an attentuation step, said
      second stage stepping said attenuation from a
      predetermined starting value to said intermediate
      value.

20.   The attenuator of Claim 19 wherein said attenuator
of said first stage responds to a first set of control
bits and said attenuator of said second stage responds to
a second set of control bits received by said attenuator.

21. The attenuator of Claim 20 wherein an attenuation of
said second stage is fixed at said intermediate value
when a one of said first set of control bits is received
by said attenuator.

5   22. The attenuator of Claim 19 wherein each said tapped
resistor comprises:
         a plurality of resistors coupled in series, a said
tap disposed between selected pairs of said resistors,
values of said resistors predetermined to provide a
10   predetermined voltage at each said tap; and
         a decoder for selectively coupling a said tap to
said non-inverting input of a said amplifier of a
corresponding stage.

23. The attenuator of Claim 20 wherein said decoder
15   comprises a plurality of decoding circuits each for
controlling a corresponding one of said taps, each said
circuit comprising:
         output drive circuitry;
         a plurality of transistors coupled in series for
20   selectively activating and deactivating a corresponding
decoder output line through said output drive circuitry;
and
         a plurality of inverters selectively coupled to
gates of said transistors such that said transistors
25   activate said corresponding output upon receiving an
assigned subset of a selected one of said first and
second sets of bits.

24. A method of resetting a audio processing system, the processing system having a plurality of registers including a reset register for receiving and storing a reset bit, a synchronization input for

5   receiving a synchronization signal, a data output for transmitting a stream of bit clocks partitioned into frames, and a clock output, the method comprising the steps of:

    setting a bit in the reset register to a first logic

10   state;

    maintaining a synchronization signal at the synchronization input in a first logic state for a preselected amount of time;

    detecting the synchronization signal after

15   expiration of said preselected amount of time;

    transitioning the synchronization signal to a second logic state;

    resetting the bit in the reset register to a second logic state;

20   initiating output of a clock from said clock output for a preselected minimum number of clocks periods after said step of transitioning; and

    detecting a valid synchronization signal for a preselected number of frames.

25   25. The method of Claim 24 wherein the audio processing system comprises a Codec.

26. The method of Claim 24 and further comprising the step of freezing a current state of at least some of the registers after said step of transitioning.

27. The method of Claim 24 and further comprising the step, subsequent to said step of detecting the validity of the synchronization signal, of setting the system in a normal operating mode, with the plurality of registers set as before said step of setting a bit in the reset register.

28. The method of Claim 24 and further comprising the step of activating detect circuitry for detecting a valid synchronization signal.

29. The method of Claim 24 wherein the preselected minimum number of clock periods comprises 2 bit clock periods.

30. The method of Claim 24 and further comprising the step of setting a system ready bit when a valid synchronization signal has been detected for two consecutive frames.

31. The method of Claim 24 wherein said steps of setting and resetting comprises the steps of setting and resetting the reset register from an audio controller.

32. The method of Claim 24 wherein said step of maintaining the synchronization signal comprises the step of maintaining the synchronization signal using an audio controller.

33.   A method of detecting a loss of synchronization in
an audio processing system, the system including an input
port for receiving data and a synchronization signal,
digital data output port for transmitting digital data,
5   and at least one analog output for transmitting analog
output data, the at least one output controlled by mute
controls, the method comprising the steps of:
        receiving the synchronization signal;
        detecting the loss of the synchronization signal;
10   enabling the mute controls controlling at least one
analog output port;
        setting the digital data out at a first logic level
until synchronization is restored;
        detecting a first active transition of a
15   synchronization signal presented to the synchronization
input;
        detecting second and third subsequent valid active
transitions of the synchronization signal; and
        disabling the mute controls of at least one analog
20   output after the third valid transition has been
detected.

34.   The method of Claim 33 and further comprising the
step of resetting the system ready bit active after the
third valid transition has been detected, and outputting
25   the system ready bit on a line of the digital port.

35.   The method of Claim 33 wherein the system includes
at least one mixer control register and the method
further comprises the step of freezing a state of the
data stored in the at least one mixer register after said
30   step of detecting a loss of synchronization.

36.   The method of Claim 33 wherein digital data
presented to the input port is discounted after said step
of detecting loss of synchronization.

37.   The method of Claim 33 and further comprising the
5   step of resuming normal operation of the system after
said step of detecting the subsequent valid
synchronization signals.

38.   The method of Claim 37 wherein normal operation is
resumed on a frame subsequent to a frame containing the
10   third valid transition.

39.   The method of Claim 33 wherein the system comprises
an audio Codec.

40.   The method of Claim 33 wherein the synchronization
signal is presented to the system by an audio controller.

CIRCUITS AND METHODS FOR IMPLEMENTING
AUDIO CODECS AND SYSTEMS USING THE SAME

ABSTRACT OF THE DISCLOSURE

5

10
Audio data processing circuitry 300 includes a plurality of analog inputs 101 for receiving analog audio data and a digital input 105 for receiving digital audio data. A analog mixer 312 mixes analog data received at said plurality of analog inputs 101 to generate a mixed analog audio stream. An analog-to-digital converter 313 converts the mixed analog audio stream to a digital audio stream and a digital mixer 315 mixes digital data received at the digital input 105 with the digital audio stream from the analog mixer 312 to generate a mixed digital audio stream.

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TABLE 1

Slot #	Definition
0	Tag/Control Information
1	Command Address Port
2	Command Data Port
3	PCM Playback Left Data
4	PCM Playback Right Data
5-12	Reserved

TABLE 1

TABLE 2

Bit #	Definition
19	Read/Write Command
18-12	Control Register Index
11-0	Reserved

TABLE 3

Slot #	Definition
0	Tag/Control Information
1	Status Address Port
2	Status Data Port
3	PCM Record Left Data
4	PCM Record Right Data
5-12	Reserved

TABLE 4

Bit #	Definition
19	Reserved (return 0)
18-12	Control Register Index
11-0	Reserved (return 0's)

TABLE 5

Reg Num	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0150h
02h	Master Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
04h	Alternate Line Out Volume	Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0	8000h
08h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	x000h
0Ch	Phone Volume	Mute	X	X	X	X	X	X	X	X	X	GN5	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	GN5	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	Aux Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Vol	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
1Eh	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
20h	General Purpose	0	0	0	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0	0000h
22h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
24h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
26h	Powerdown Ctrl/Stat	0	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC	0000h
28h	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..	..
5Ah	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XXXXh
..																		..
76h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XXXXh
78h	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XXXXh
7Ah	Reserved	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	XXXXh
7Ch	Vendor ID1(CR)	0	1	0	0	0	0	1	1	0	1	0	1	0	0	1	0	4352h
7Eh	Vendor ID2(Y1)	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	1	5901h

TABLE 6

Gx4 - Gx0	Gain Level
0000	+12 dB
0001	+10.5 dB
...	...
00111	+1.5 dB
0100	0 dB
0101	-1.5 dB
...	...
11111	-34.5 dB

Analog Mixer Input Gain Values

TABLE 7

3x2 - 3x0	Record Source
0	MIC
1	CD Input
2	Video Input
3	AUX Input
4	Line Input
5	Stereo Mix
6	Mono Mix
7	Phone Input

Input Mux Selection Options

TABLE 8

Gx3 - Gx0	Gain
1111	+22.5 dB
0000	0 dB

Input Mux Selection Options

TABLE 9

Bit Name	Function
REF	Vref at nominal levels
ANL	Analog Mixers, Mux, and Volume Controls ready
DAC	DAC ready to accept data
ADC	ADC ready to transmit data

Codec Powerdown Status Bits

TABLE 10

Bit Name	Function
PR0	ADCs and Input Mux Powerdown
PR1	DACs Powerdown
PR2	Analog Mixer Powerdown (Vref still on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	AC-Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disable
PR6	Alternate Line Output Buffer Powerdown

Codec Powerdown Control Bits

TABLE 11

A1-A0	ADC Accessed
0	None
1	ADC Main Left Channel .
2	ADC Main Right Channel
3	Reserved

ADC Calibration Register Address Mapping

TABLE 12

D1-D0	DAC Accessed
0	None
1	DAC Main Left Channel
2	DAC Main Right Channel
3	Reserved

DAC Calibration Register Address Mapping

TABLE 13

PR Bit	Function
PR0	Main ADC's and Input Mux Powerdown
PR1	Main DAC's Powerdown
PR2	Analog Mixer Powerdown (Vref on)
PR3	Analog Mixer Powerdown (Vref off)
PR4	AC-Link Powerdown (BIT_CLK off)
PR5	Internal Clock Disable (lockup)
PR6	Alternate Line Out Buffer Powerdown

Powerdown GPR Bit Functions

TABLE 14

PDN Signal	PR0	PR1	PR2	PR3	PR4	PR5	PR6	Equation
PDN_DAC	X	1	1	1	X	1	X	PR1+PR2+PR3+PR5
PDN_ADC	1	X	X	1	X	1	X	PR0+PR3+PR5
PDN_MIX	X	X	1	1	X	1	X	PR2+PR3+PR5
PDN_REF	X	X	X	1	X	1	X	PR3+PR5
PDN_BITCLK	X	X	X	X	1	1	X	PR4+PR5
PDN_ALT_LINE	X	X	1	1	X	1	1	PR2+PR3+PR5+PR6
PDN_CLK256_INT	X	X	X	X	X	1	X	PR5

Powerdown Control Signals

TABLE 15

Test Mode	Test Name
0	None - normal operation
1	ADC 1-bit Left Channel Data Test
2	ADC 1-bit Right Channel Data Test
3	DAC 1-bit Left Channel Data Test
4	DAC 1-bit Right Channel Data Test
5	Analog and Digital Wrap Test
6	Disable Zero-Cross Detect
7	Zero Cross Detect Test
8	Test Slow Counters
9	Test OpAmps
10	NAND Tree Enabled
11	Disable Calibration
12	Force OPAMP Calibration
13	Force ADC Calibration
14	Force DAC Calibration
15	Enable Calibration Register Writes

TABLE 16

Op-Amp	Output Enable Bit	Mixer Register Bit
PC_BEEP	LSB of attn bits	Bit D1 of Register 0xa
PHONE	LSB of gain/attn bits	Bit D0 of Register 0xC
PCM_OUT_LEFT	LSB of gain/attn bits	Bit D8 of Register 0x18
PCM_OUT_RIGHT	LSB of gain/attn bits	Bit D0 of Register 0x18
MIC_BOOST	0/20 dB Control Bit	Bit D6 of Register 0xE
MIC	LSB of gain/attn bits	Bit D0 of Register 0xE
LINE_LEFT	LSB of gain/attn bits	Bit D8 or Register 0x10
LINE_RIGHT	LSB of gain/attn bits	Bit D0 of Register 0x10
CD_LEFT	LSB of gain/attn bits	Bit D8 of Register 0x12
CD_RIGHT	LSB of gain/attn bits	Bit D0 of Register 0x12
VIDEO_LEFT	LSB of gain/attn bits	Bit D8 of Register 0x14
VIDEO_RIGHT	LSB of gain/attn bits	Bit D0 of Register 0x14
AUX_LEFT	LSB of gain/attn bits	Bit D8 of Register 0x16
AUX_RIGHT	LSB of gain/attn bits	Bit D0 of Register 0x16
ADC_INMUX_LEFT	CD_LEFT_SEL	Bit D8 of Register 0x1A
ADC_INMUX_RIGHT	CD_RIGHT_SEL	Bit D0 of Register 0x1A
ADC_INGAIN_LEFT	LSB of gain bits	Bit D8 of Register 0x1C
ADC_INGAIN_RIGHT	LSB of gain bits	Bit D0 of Register 0x1C
Analog Input Mixer Left	NMUTE_LINE_L	Bit D15 of Register 0x10
Analog Input Mixer Right	NMUTE_CD_L	Bit D15 of Register 0x12
Analog Output Mixer Left	NMUTE_PHONE	Bit D15 of Register 0xC
Analog Output Mixer Right	NMUTE_MIC	Bit D15 of Register 0xE
MONO_OUT Stereo to Mono Mixer	NMUTE_VIDEO_L	Bit D15 of Register 0x14
ADC_INMUX Stereo to Mono Mixer	NMUTE_AUX_L	Bit D15 of Register 0x16
LINE_OUT_LEFT First Stage	LSB of attn bits	Bit D8 of Register 0x2
LINE_OUT_RIGHT First Stage	LSB of attn bits	Bit D0 of Register 0x2
LINE_OUT_LEFT Second Stage	Bit 1 of attn bits	Bit D9 of Register 0x2
LINE_OUT_RIGHT Second Stage	Bit 1 of attn bits	Bit D1 of Register 0x2
ALT_LINE_OUT_LEFT First stage	LSB of attn bits	Bit D8 of Register 0x4
ALT_LINT_OUT_RIGHT First Stage	LSB of attn bits	Bit D0 of Register 0x4
ALT_LINE_OUT_LEFT Second Stage	Bit 1 of attn bits	Bit D9 of Register 0x4
ALT_LINE_OUT_RIGHT Second Stage	Bit 1 of attn bits	Bit D1 of Register 0x4
MONO_OUT First Stage	LSB of attn bits	Bit D0 of Register 0x6
MONO_OUT Second Stage	Bit 1 of attn bits	Bit D1 of Register 0x6

TABLE 17

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	DVdd1	17	VIDEO_R	33	nc
2	XTL_IN	18	CD_L	34	nc
3	XTL_OUT	19	CD_GND	35	LINE_OUT_L
4	DVss1	20	CD_R	36	LINE_OUT_R
5	SDATA_OUT	21	MIC1	37	MONO_OUT
6	BIT_CLK	22	MIC2	38	AVdd2
7	DVss2	23	LINE_IN_L	39	ALT_LINE_OUT_L
8	SDATA_IN	24	LINE_IN_R	40	nc
9	DVdd2	25	AVdd1	41	ALT_LINE_OUT_R
10	SYNC	26	AVss1	42	AVss2
11	RESET#	27	RefFlt	43	nc
12	PC_BEEP	28	Vref	44	nc
13	PHONE	29	AFILT1	45	nc
14	AUX_L	30	AFILT2	46	nc
15	AUX_R	31	nc	47	nc
16	VIDEO_L	32	nc	48	nc

TABLE 18

Signal Name	I/O	Description
XTL_IN	I	24.576 MHz Crystal Input
XTL_OUT	O	24.576 MHz Crystal Output
BIT_CLK	O	12.288 MHz Serial Data Clock
SYNC	I	48 kHz Sample Sync Clock
SDATA_OUT	I	Serial AC'97 Input Stream
SDATA_IN	O	Serial AC'97 Output Stream
RESET#	I	Asynchronous AC'97 HW Reset

TABLE 19

Signal Name	I/O	Description
PC_BEEP	I	PC Speaker Beep
PHONE	I	From Telephone Speakerphone
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE_IN_L	I	Line In Left Channel
LINE_IN_R	I	Line In Right Channel
CD_L	I	CD Audio Left Channel Input
CD_GND	I	CD Audio Analog Ground
CD_R	I	CD Audio Right Channel Input
VIDEO_L	I	Video Audio Left Channel Input
VIDEO_R	I	Video Audio Right Channel Input
AUX_L	I	Auxiliary Left Channel Input
AUX_R	I	Auxiliary Right Channel Input
LINE_OUT_L	O	Line Out Left Channel
LINE_OUT_R	O	Line Out Right Channel
ALT_LINE_OUT_L	O	Alternate Line Out Left Channel
ALT_LINE_OUT_R	O	Alternate Line Out Right Channel
MONO_OUT	O	To Telephony Speakerphone

TABLE 20

Signal Name	I/O	Description
REFFLT	O	Reference Voltage Filter
VREF	O	Reference Voltage Output
AFILT1	O	Main Left ADC Filter Cap
AFILT2	O	Main Right ADC Filter Cap

Table 21: Bonnie Filter and Reference Voltages

TABLE 21

Signal Name	I/O	Description
AVdd1	I	Analog Vdd - 5.0V
AVdd2	I	Analog Vdd - 5.0V
AVdd3	I	Analog Vdd - 5.0V
AVss1	I	Analog Ground
AVss2	I	Analog Ground
AVss3	I	Analog Ground
DVdd1	I	Digital Vdd - 5.0V or 3.3V
DVdd2	I	Digital Vdd - 5.0V or 3.3V
DVss1	I	Digital Ground
DVss2	I	Digital Ground

TABLE 22

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage range	Vin	-0.30	-	DVdd + 0.30	V
Low Level Input Voltage	Vil	-	-	0.30 ° Vdd	V
High Level Input Voltage	Vih	0.40 ° Vdd	-	-	V
High Level Output Voltage	Voh	0.60 ° Vdd	-	-	V
Low Level Output Voltage	Vol	-	-	0.10 ° Vdd	V
Input Leakage Current (AC-Link Inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z AC-Link Outputs)	-	-10	-	10	uA
Output Buffer Drive Current	-	-	5	-	mA

TABLE 23

AC CHARACTERISTICS (Standard test conditions unless otherwise noted: $T_{ambient} = 25^0 C$, AVdd = DVdd = 5.0 V +/- 5%; Input Voltage Levels: Logic Low = 0.8V, Logic High = 2.4V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0dB = 1Vrms, 10kW/50pF load (Note 1) This data is preliminary.

Parameter		Min	Typ	Max	Units
Full Scale Input Voltage:					V_{rms}
Line Inputs		-	1.0	-	
Mic Inputs	(Note 3)	-	0.1	-	
Full Scale Output Voltage:					V_{rms}
Line Output		-	1.0	-	
Headphone Output (Alternate Line Output)		-	1.0	-	
Analog S/N:					dB
CD to LINE_OUT		90	-	-	
Other to LINE_OUT		-	85	-	
Analog Frequency Response	(Note 4)	20	-	20,000	Hz
Digital S/N	(Note 5)				dB
D/A	(Note 2)	80	0.1	-	
A/D		80	0.1	-	
Total Harmonic Distortion:					%
Line Output	(Note 6)	-	-	-	
Headphone Output (Alternate Line Output)		-	-	-	
D/A & A/D Frequency Response	(Note 7)	20	-	19,200	Hz
Transistion Band		$0.4 F_s$	-	$0.6 F_s$	Hz
Stop Band		$0.6 F_s$	-	-	Hz
Stop Band Rejection	(Note 8)	74	-	-	dB
Out-of-Band Energy	(Note 9)	-	-	-45	dB
Group Delay	(Note 2)	-	-	1	ms
Power Supply Rejection Ratio (1KHz)	(Note 2)	40	-	-	dB
Interchannel Isolation		-	80	-	dB
Spurious Tone Reduction		-	-100	-	dB
Attenuation, Gain Step Size		-	1.5	-	dB
Input Impedance	(Note 2)	10	-	-	kΩ
External Load Impedance	(Note 2)	10			kΩ
Input Capacitance	(Note 2)	-	15	-	pF
Vrefout		-	2.2	-	V

Notes:
3. With +20dB Boost on, 1.0Vrms with Boost off
4. ±1dB limits Analog frequency response refers to analog signal paths only. No digital signal paths are included
5. The ratio of the rms output level with 1KHz full scale input to the rms output level with all zeros into the digital input. Measured "A wtd" over a 20Hz to a 20KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. -3 dB gain, 20 KHz BW, 48 KHz Sample Frequency
7. +-0.25 dB limits
8. Stop Band rejection determines filter requirements. Out-of-band rejection determines audible noise.
9. The integrated Out-of-Band generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8kHz to 100 kHz, with respect to a $1V_{RMS}$ DAC output.

TABLE 24

SELECT VALUE	Stage 1	Stage 2	Attenuation Total
0 0 0 0 0 0	0dB	0dB	0 dB
0 0 0 0 0 1	0dB	-1.5dB	-1.5d
⋮	⋮	⋮	
0 1 1 1 1 1	0dB	-46.5 dB	-46.5 dB
1 0 0 0 0 0	0dB	-48dB	-48dB
1 0 0 0 0 1	-1.5dB	-48dB	-49.5dB
⋮	⋮	⋮	
1 1 1 1 1 1	-46.5dB	-48 dB	-94.5 dB

Input Sources
4 Mono
4 Stereo

101

Output Sources
1 Mono
2 Stereo

107

100

8

3

Σ

106

102

ADCs

103

DACs

106

AC-link

104

5

105

5 wire
Serial link

FIG. 1A

FIG. 1B

Powered
Speakers
(10KΩ) 201

Alternate
Analog
(10KΩ)
202

Headphones
(32Ω)
203

Telephone
Receiver 204

2/

2/

2/

2/

LINE OUT

ALT LINE OUT

HP OUT

PHONE

Codec
100

SYNC

BIT_CLK

SDATA_OUT

SDATA_IN

RESET#

AC'97
DIGITAL
CONTROLLER
200
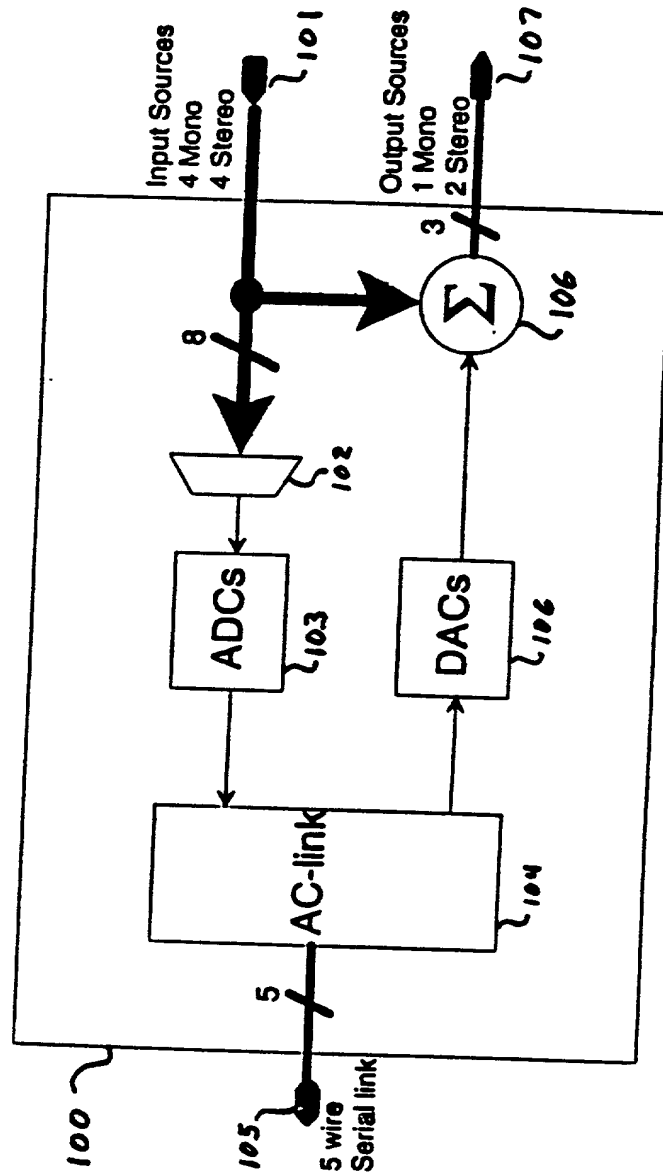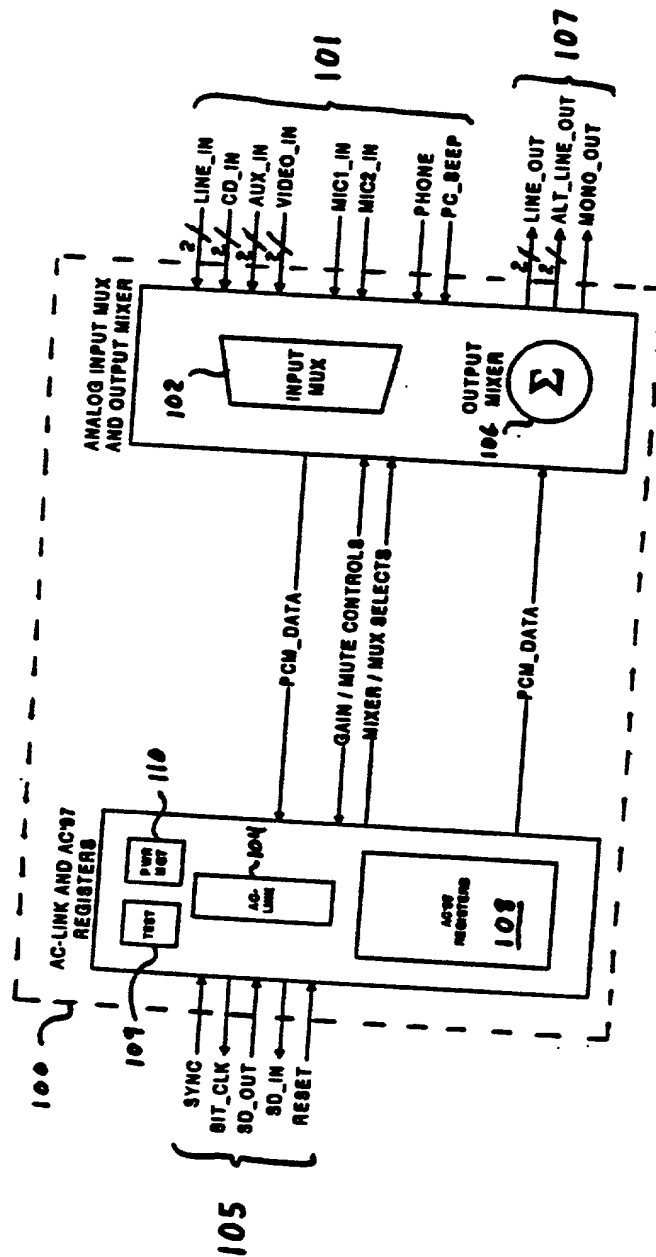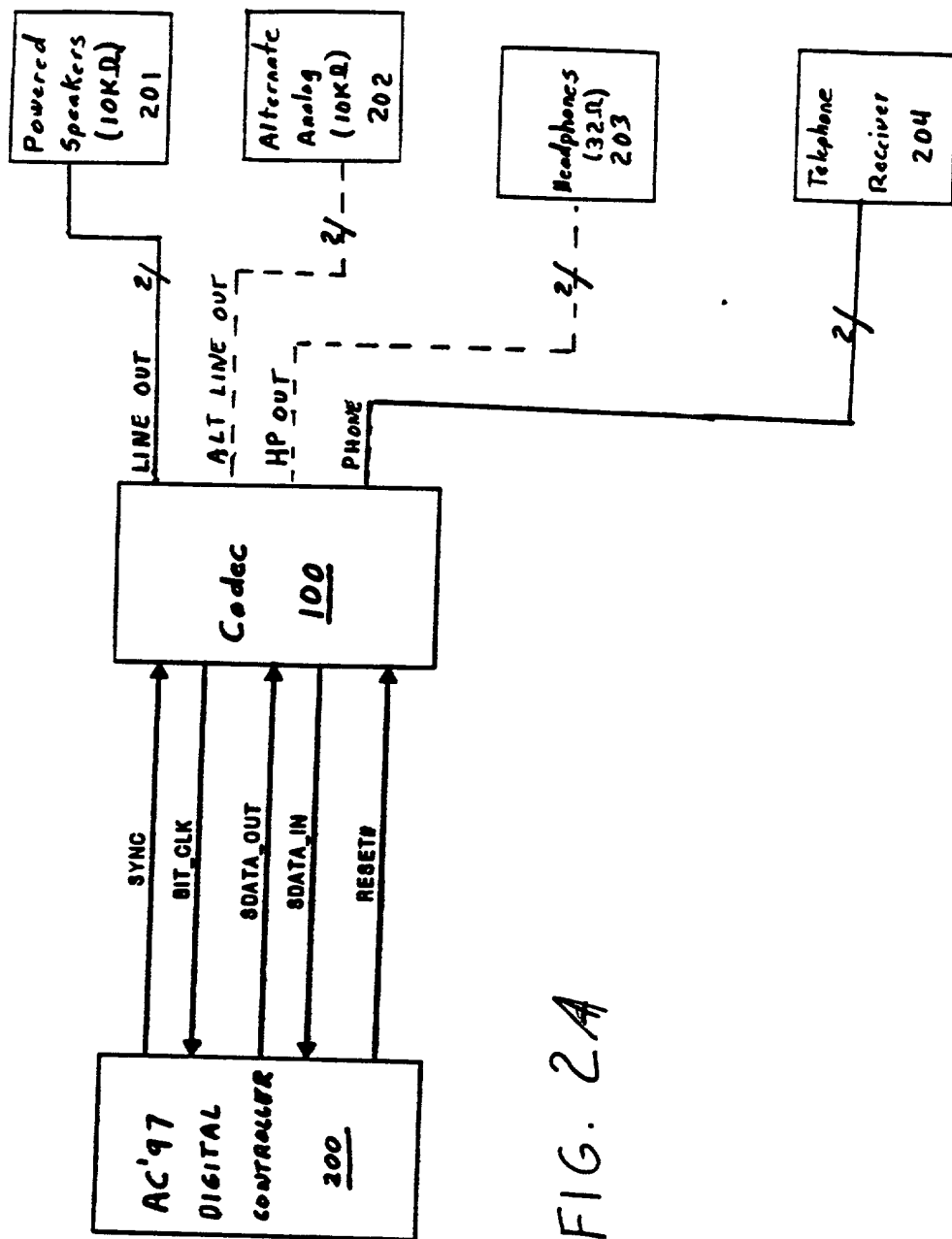
FIG. 2A

FIG. 2B

0   1   2   3   4   5   6   7   8   9   10   11   12

16 bit slots

| TAG |

16	20	20	20	20	20	20	20	20	20	20	20	20
TAG	CMD ADDR	CMD DATA	PCM LEFT	PCM RIGHT	OPT. MODEM	RES.	RES.	RES.	RES.	RES.	RES.	RES.

16	20	20	20	20	20	20	20	20	20	20	20	20
TAG	STATUS ADDR	STATUS DATA	PCM LEFT	PCM LEFT	OPT. MODEM	OPT. MIC	RES	RES	RES	RES.	RES.	RES.

FIG. 3A

FIG. 3B
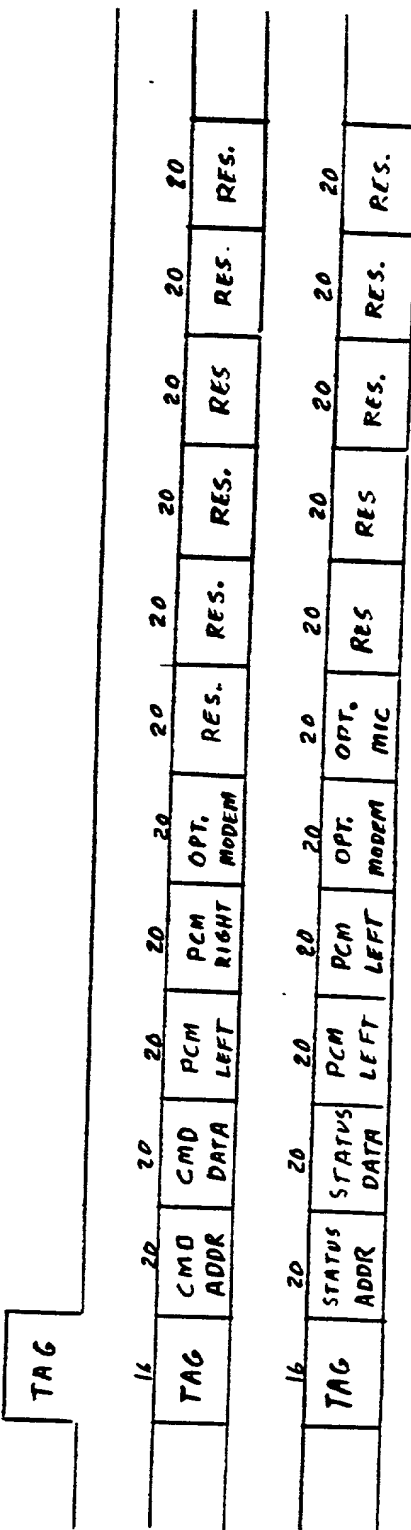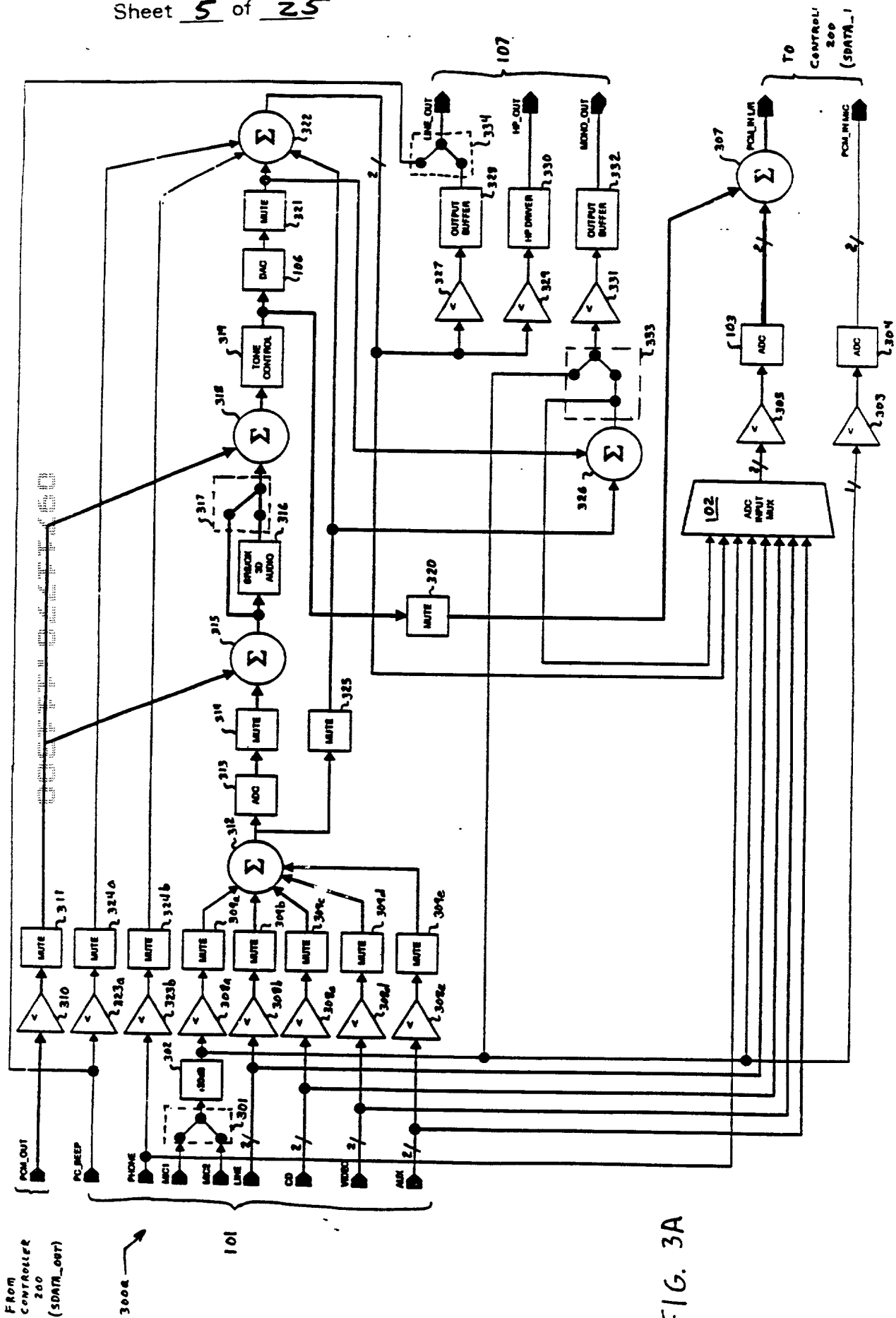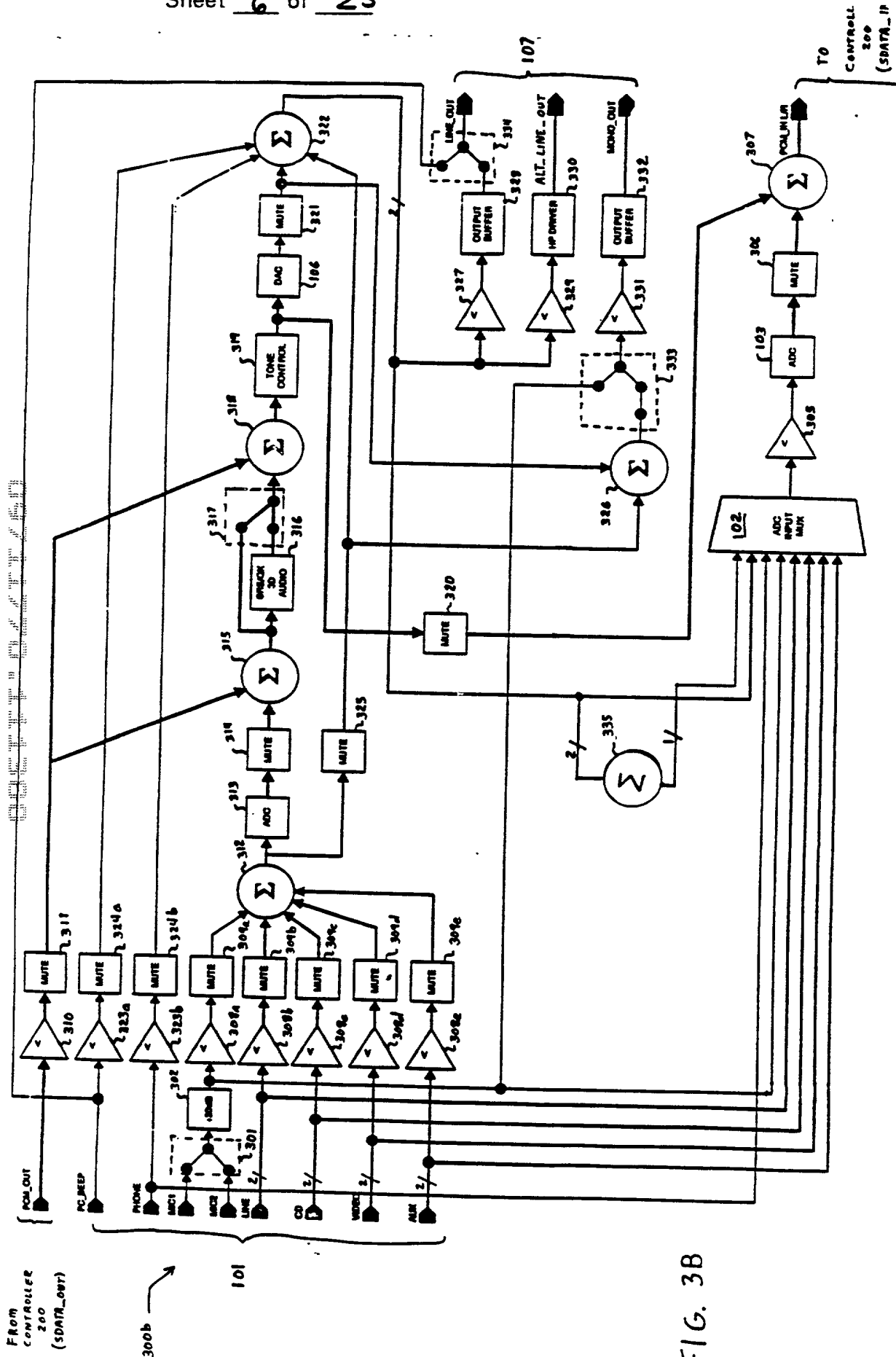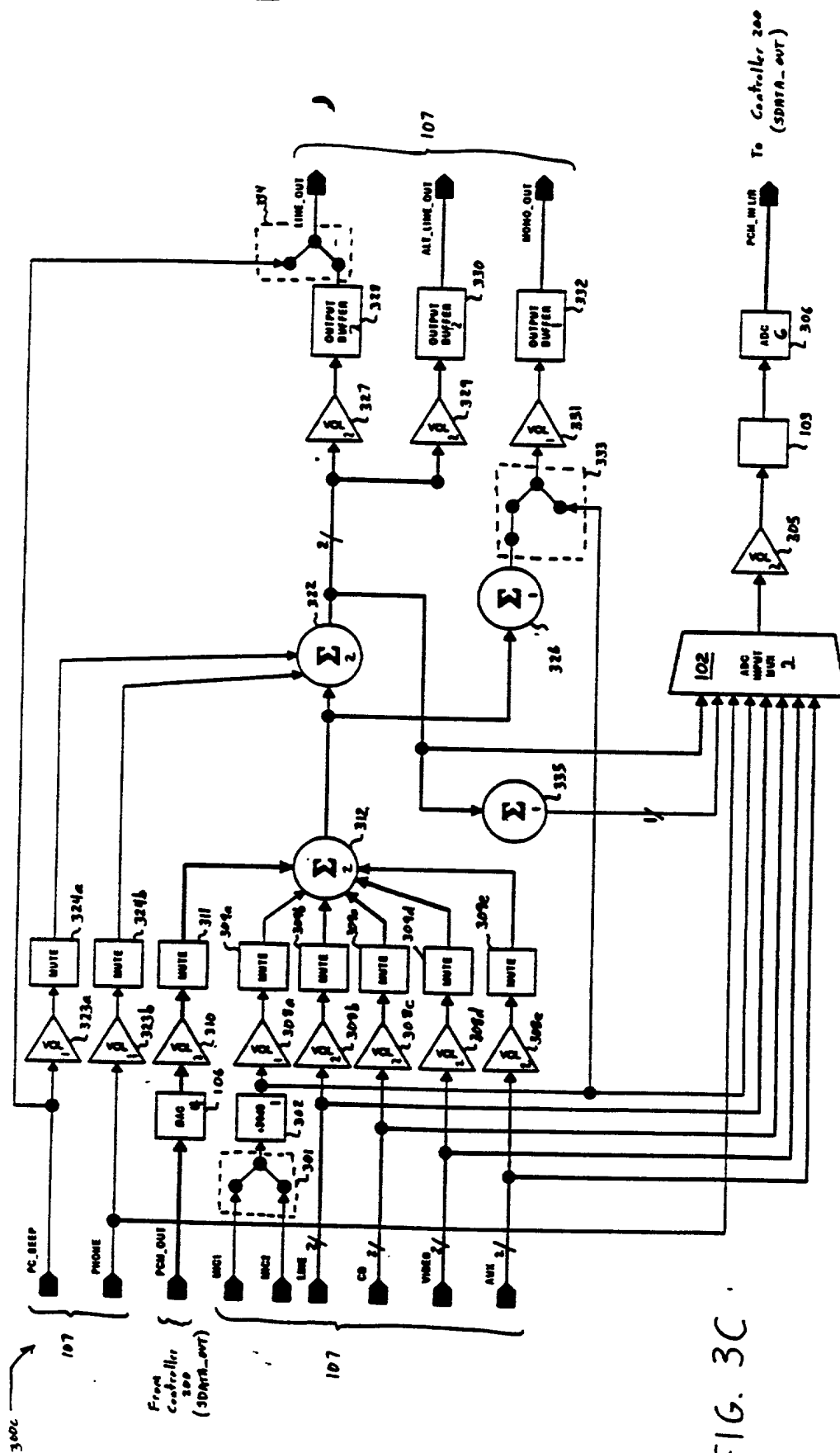
FIG. 3C

FIG. 4A

Master Volume (Index 02h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0

FIG. 4b

Alternate Volume (Index 04h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	X	ML5	ML4	ML3	ML2	ML1	ML0	X	X	MR5	MR4	MR3	MR2	MR1	MR0

FIG. 4c

Master Mono Volume (Index 06h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	X	X	X	X	X	X	X	X	X	MM5	MM4	MM3	MM2	MM1	MM0

FIG. 4d

PC_BEEP Volume (Index 0Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X

FIG. 4e

Analog Mixer Input Gain Registers (Index 0C - 18h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Mute	X	X	Gx4	Gx3	Gx2	Gx1	Gx0	X	X	X	Gx4	Gx3	Gx2	Gx1	Gx0

FIG. 4G

General Purpose Register (Index 20h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	MIX	MS	LPBK	0	0	0	0	0	0	0

FIG. 4H

Powerdown Control/Status Register (Index 26h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	PR6	PR5	PR4	PR3	PR2	PR1	PR0	0	0	0	0	REF	ANL	DAC	ADC

FIG. 4I

Test Control Register (Index 5Ch)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	T3	T2	T1	T0

FIG. 4J

ADC/DAC Calibration Address Register (Index 76h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
WEA	0	0	0	0	0	A1	A0	WED	0	0	0	0	0	D1	D0

FIG. 4K

ADC Calibration Data Register (Index 78h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIG. 4L

DAC Calibration Data Register (Index 7Ah)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

FIG. 5

insync_st = 0

exsync = isync & count = 8'd255

isync_st = 1

count = 8'd255

insync_st = 3

IN

ENABLE

ZCD 604

601a

603a

602a

+ −

Vcn

601b

603b

602b

+ −

Vcn

OUT

FIG. 6A

FIG. 6B

FIG. 6C

OUT

V_{dd} ~615

~616a

~616b

V_{dd} ~614

~613a

~613b

~611a

~611b

~611c

~611d

~611e

~611f

~612

Pdb

610a

610b

610c

610d

610e

610f

FIG. 6D

FIG. 7

MIXER_REG_MUTE —
NO_SYNC_MUTE — ⟩— To Mute Control

FIG. 8

48-PIN TQFP (KQ)

Pins (left side, top to bottom): 37 MONO_OUT, 38 AVdd2, 39 ALT_LINE_OUT_R, 40 NC, 41 ALT_LINE_OUT_R, 42 AVss2, 43 NC, 44 NC, 45 NC, 46 NC, 47 NC, 48 NC

Pins (bottom side, left to right): 1 DVdd1, 2 XTL_IN, 3 XTL_OUT, 4 DVss1, 5 SDATA_OUT, 6 BIT_CLK, 7 DS$_{ss}$2, 8 SDATA_IN, 9 DVdd2, 10 SYNC, 11 RESET, 12 PC_BEEP

Pins (right side, top to bottom): 24 LINE_IN_R, 23 LINE_IN_L, 22 MIC2, 21 MIC1, 20 CD_R, 19 CD_GND, 18 CD_L, 17 VIDEO_R, 16 VIDEO_L, 15 AUX_R, 14 AUX_L, 13 PHONE

Pins (top side, left to right): 36 L_OUT_R, 35 L_OUT_L, 34 NC, 33 NC, 32 NC, 31 NC, 30 AFLT2, 29 AFLT1, 28 Vrefout, 27 REFFLT, 26 AVss1, 25 AVdd1

DECLARATION AND POWER OF ATTORNEY

As below named inventors, we declare that:

Our residences, post office addresses and citizenships are as stated below next to our names, that we believe we are the original and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention or design e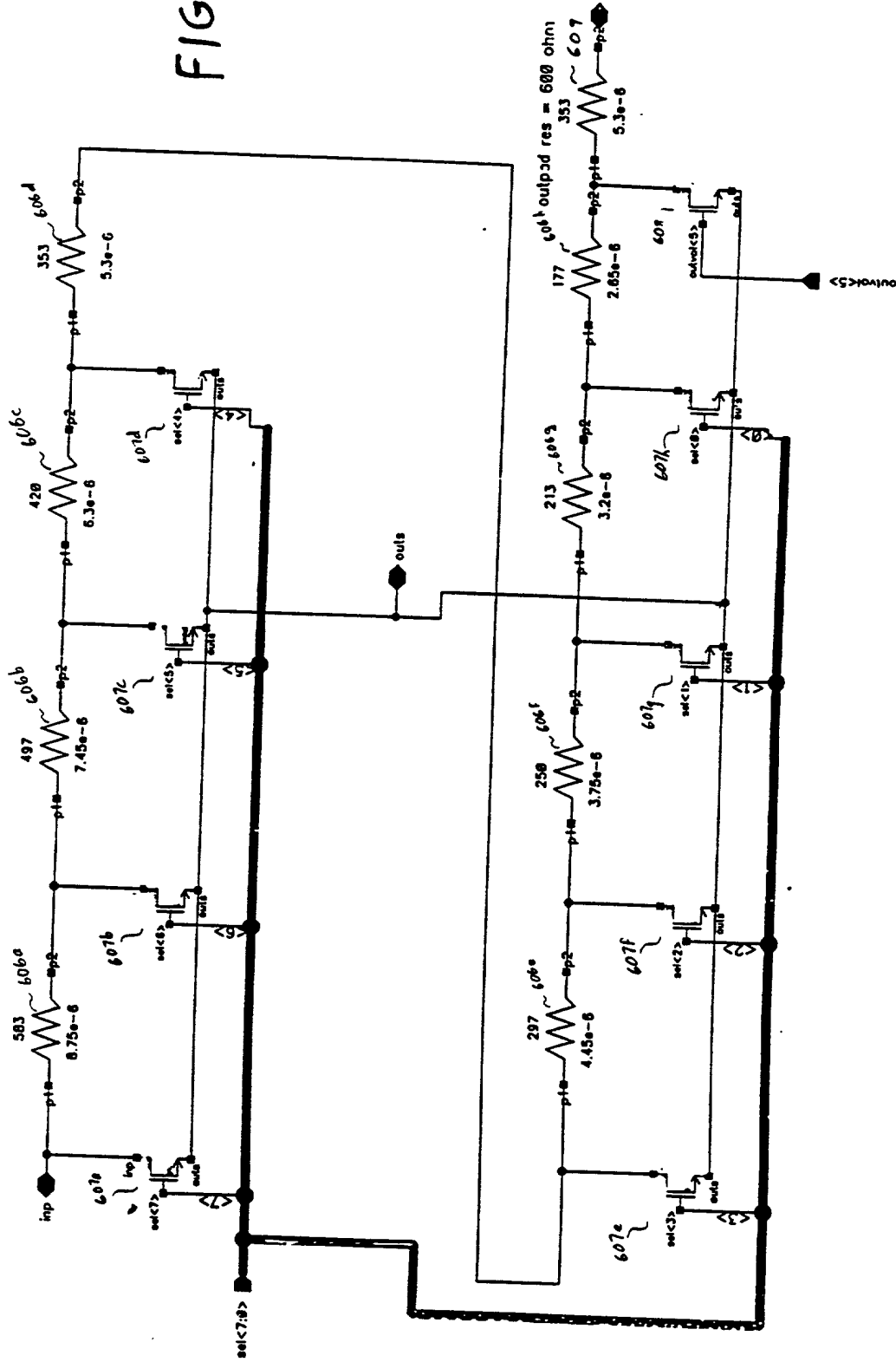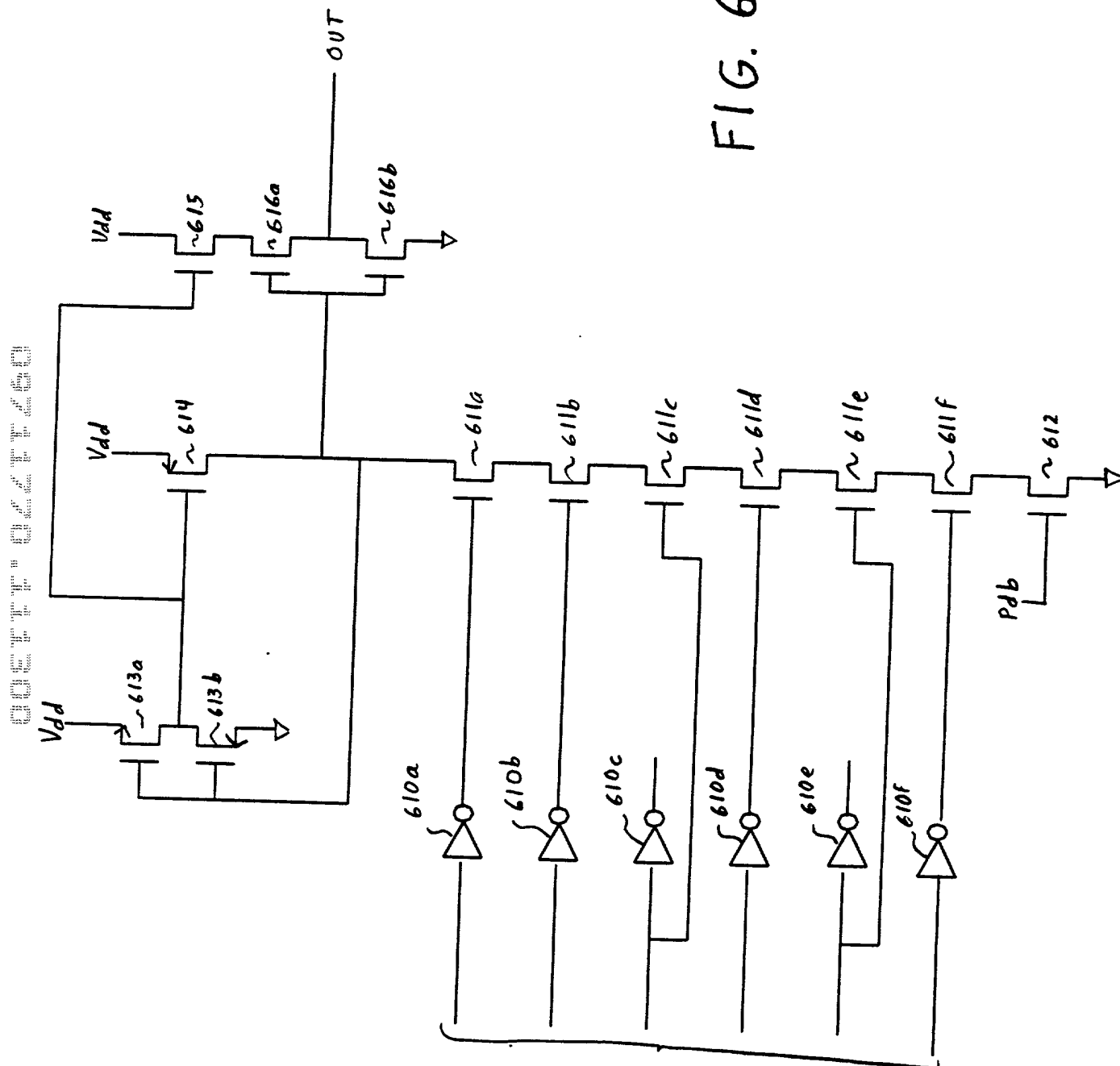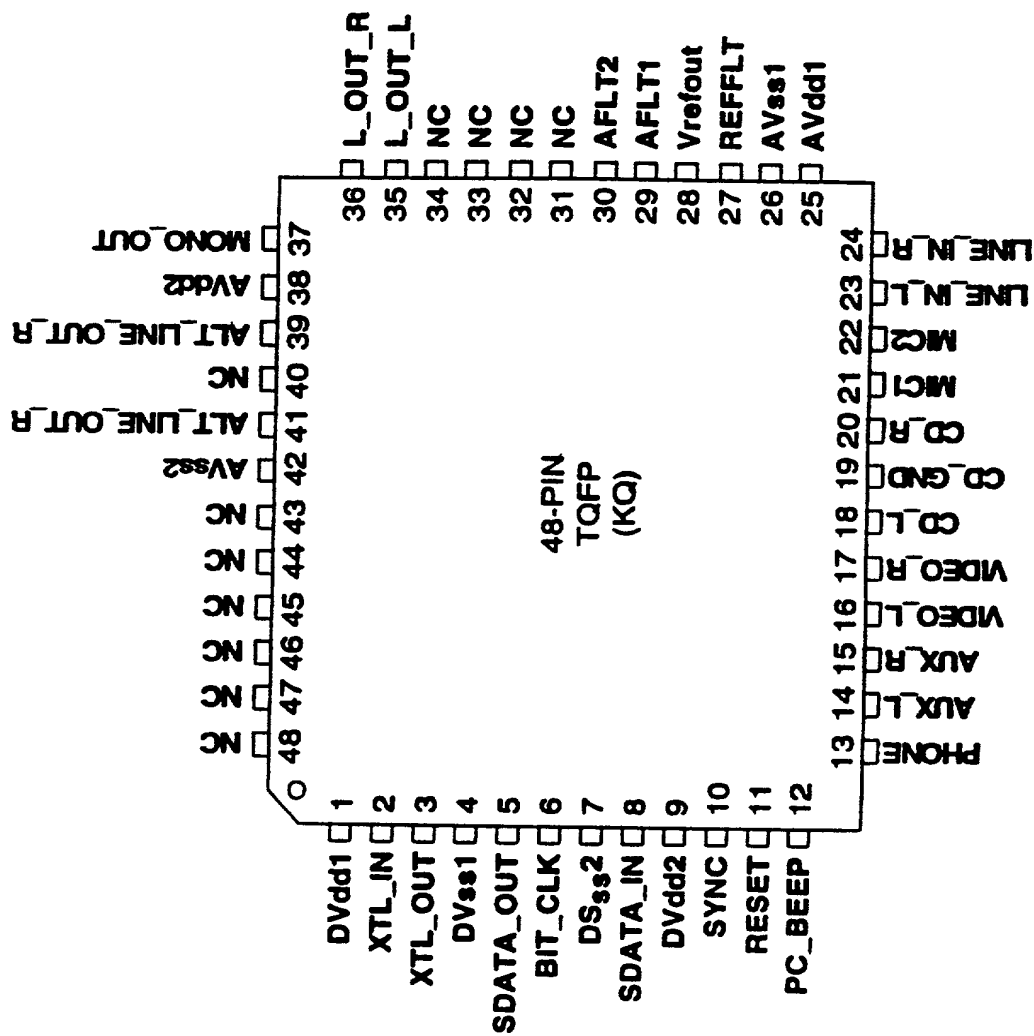ntitled **"CIRCUITS AND METHODS FOR IMPLEMENTING AUDIO CODECS AND SYSTEMS USING THE SAME"** specification of which was filed April 4, 1997 and assigned U.S. Serial No. 08/833,195; that we have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above; and that we acknowledge our duty to disclose information known to be material to the patentability of a pending claim in this application in accordance with 37 C.F.R. 1.56(a).

We hereby claim the benefit under Title 35 United States Code § 120 of any United States application(s) listed below and, insofar as any subject matter of any claim of this application is not disclosed in the prior United States Application, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application: N/A

Serial No.	Filing Date

We hereby appoint:

Gregory W. Carr	Reg. No. 31,093
Philip T. Golden	Reg. No. 37,631
Elizabeth R. Hall	Reg. No. 37,344
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of the firm of Winstead Sechrest & Minick P.C. and Cirrus
Logic, Inc., our attorneys with full power of substitution and
revocation, to prosecute this application and to transact all
business in the United States Patent and Trademark Office
connected therewith, and to file and prosecute any
international patent applications filed thereon before any
international authorities under the Patent Cooperation Treaty.

Send Correspondence To: Direct Telephone Calls To
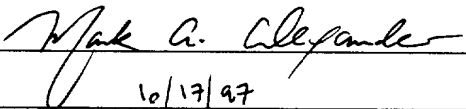
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We declare that all statements made herein of our own
knowledge are true and that all statements made on information
and belief are believed to be true; and further that these
statements were made with the knowledge that willful false
statements and the like so made are punishable by fine or
imprisonment, or both, under Section 1001 of Title 18 of the
United States Code, and that such willful false statements may
jeopardize the validity of the application or any patent
issuing thereon.

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